

B550I AORUS PRO AX

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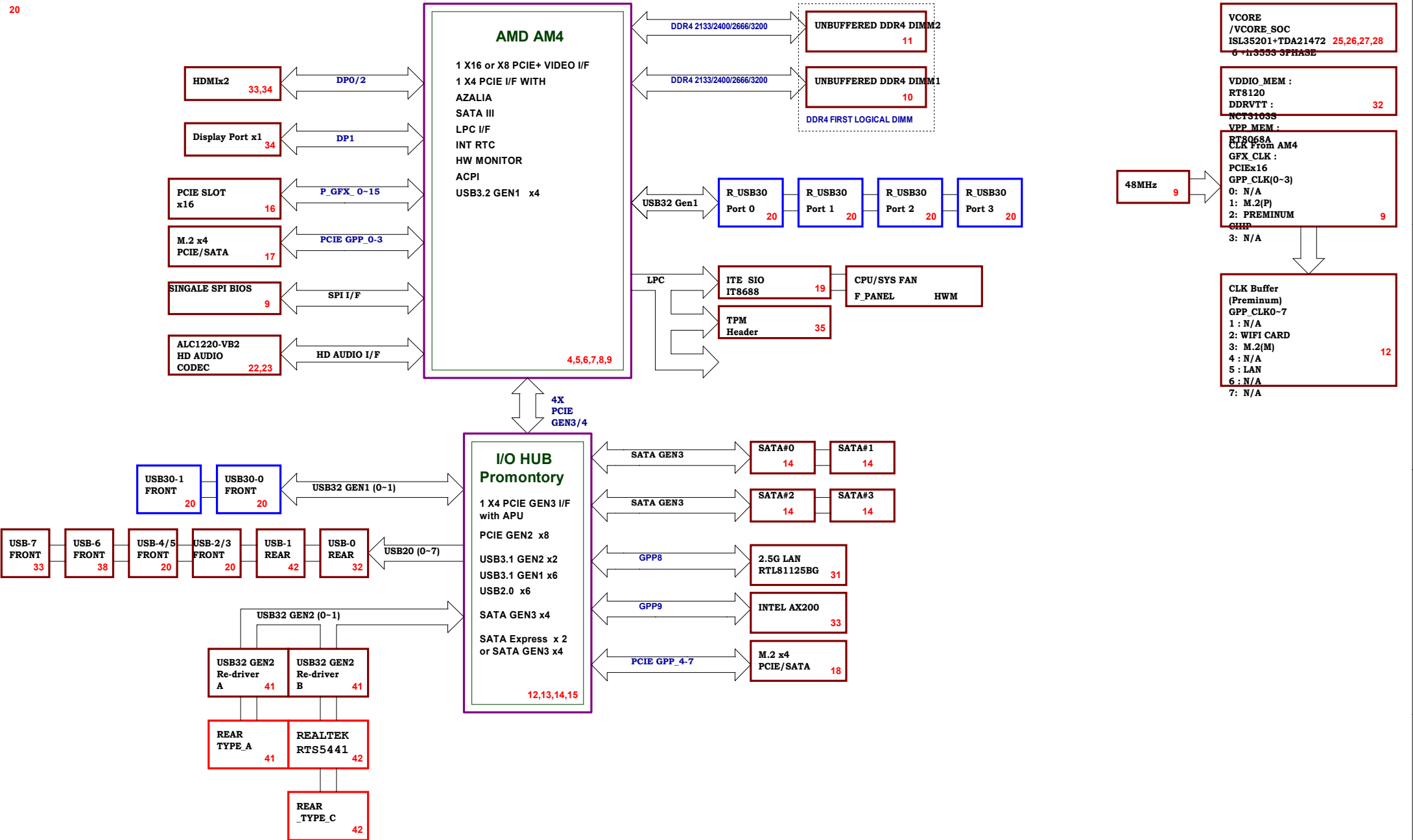
Component Value Change History

P-Code: U18038-0
DATE: 2020/05/11

Date	Change Item	Reason
2020/02/04	R0.1 SCH.	NEW B550 ITX PROJECT.
		PWM RAA229004 6+2PHASE. Q_FLASH IT5702. 2.5G LAN I225V.
2020/02/04		MODIFY 2.5G LAN TO REALTEK RTL8125.
2020/03/24	R0.2 SCH.	IT5702 料號改為10HP2-NW5702-13R,Update LED 模組Add MCUR158,
		Q-Flash 模組修改,REMOVE MCU SMBUS SWITCH,LED 改為3VDUAL,
		ADD PWM RAA229004 power sequence.
		M2B_PCH LANE0~3 CHANGE TO M2B_SB LANE4~7 support SATA MODE.
2020/03/25		Add PCIE x16 A32 Bifurcation GPIO. ADD AR8/UC56.
2020/03/27		Add INTERSIL PWM SMBUS SWITCH. MODIFY GPP PCIE SETTING.
2020/04/01		UPDATE PCH_HS/TMOS_HS/M_BIOS FOOTPRINT.
2020/04/01		Add DAC9 close to DAQ2, FIXED RTC leakage AR132 3VDUAL_IO.
2020/04/09		RTC PIN8 PULL RTCVDD3.ADD MB_ID3.
2020/04/21	R1.0 SCH.	UPDATE T5702 模組,RTC CLEAR CMOS WTD線路.
		UPDATE PWM模組,REMOVE SMBUS SWITCH,FIX VCCIO(PIN7)漏電.
		UPDATE AUDIO (Renoir Only)漏電(A_VDD1V8改為A_VDD18S5).
		C92/C225/CEC10/CEC11/CEC40/CEC11改47U/0805.
2020/04/22		0OHM-->SHORT PAD DR17/DR18/MOATAR1.REMOVE R23/R28.
2020/04/27		REMOVE AQ2. PCIEX16-->GEN4/SHELL.
2020/05/07	F_等級	REMOVE ECD_Q4(F_RESET),UPDATE U31RB_EQB-->F.
2020/05/11	F_等級	IT5702 update,ECD_Q4上件, ECD_Q5不上件.

Circuit or PCB Layout Change For Next Version

[illegible]



AM4A

MEMORY A

MAAA0	A332	MA_A0C0[0]
MAAA1	T32	MA_A0C0[1]
MAAA2	T35	MA_A0C0[2]
MAAA3	T31	MA_A0C0[3]
MAAA4	R30	MA_A0C0[4]
MAAA5	R33	MA_A0C0[5]
MAAA6	R32	MA_A0C0[6]
MAAA7	P34	MA_A0C0[7]
MAAA8	P30	MA_A0C0[8]
MAAA9	P31	MA_A0C0[9]
MAAA10	A336	MA_A0C0[10]
MAAA11	P33	MA_A0C0[11]
MAAA12	N35	MA_A0C0[12]
MAAA13	A332	MA_A0C0[13]

[10] MA_ACT-	MA_ACT-	M35	MA_ACT_L
[10] MA_BG0	MA_BG0	N31	MA_BG0[0]
[10] MA_BG1	MA_BG1	N32	MA_BG1[0]

[10] MA_BA0	MA_BA0	A335	MA_BA0[0]
[10] MA_BA1	MA_BA1	A333	MA_BA1[0]

[10] MA_DM0[0.8]	MA_DM0	K19	MA_DM0[0]
	MA_DM1	J23	MA_DM1[0]
	MA_DM2	G26	MA_DM2[0]
	MA_DM3	H30	MA_DM3[0]
	MA_DM4	A331	MA_DM4[0]
	MA_DM5	AVG1	MA_DM5[0]
	MA_DM6	AL29	MA_DM6[0]
	MA_DM7	AL26	MA_DM7[0]
	MA_DM8	G34	MA_DM8[0]

DQSA0	H19	MA_DQSA[0]
DQSA1	G19	MA_DQSA[1]
DQSA2	F23	MA_DQSA[2]
DQSA3	C33	MA_DQSA[3]
DQSA4	F27	MA_DQSA[4]
DQSA5	F26	MA_DQSA[5]
DQSA6	F30	MA_DQSA[6]
DQSA7	F30	MA_DQSA[7]
DQSA8	AJ31	MA_DQSA[8]
DQSA9	AJ33	MA_DQSA[9]
DQSA10	AJ34	MA_DQSA[10]
DQSA11	AN32	MA_DQSA[11]
DQSA12	AN33	MA_DQSA[12]
DQSA13	AP29	MA_DQSA[13]
DQSA14	AN29	MA_DQSA[14]
DQSA15	AP26	MA_DQSA[15]
DQSA16	AN26	MA_DQSA[16]
DQSA17	H34	MA_DQSA[17]
DQSA18	H33	MA_DQSA[18]

T34	MA_CLK[0]
U34	MA_CLK[1]
U33	MA_CLK[2]
V33	MA_CLK[3]

[10] MA_CLKH2	MA_CLKH2	V35	MA_CLKH2[0]
[10] MA_CLKL2	MA_CLKL2	V36	MA_CLKL2[0]
[10] MA_CLKH3	MA_CLKH3	V32	MA_CLKH3[0]
[10] MA_CLKL3	MA_CLKL3	W32	MA_CLKL3[0]

[10] MA_RST-	MA_RST-	L33	MA_RST_L
[10] MA_EVENT-	MA_EVENT-	W35	MA_EVENT_L

[10] MA1_CKE0	MA1_CKE0	M32	MA1_CKE0[0]
[10] MA1_CKE1	MA1_CKE1	M33	MA1_CKE1[0]

[10] MODT_A2	MODT_A2	AD33	MA1_C0T0[0]
[10] MODT_A3	MODT_A3	AF34	MA1_C0T0[1]

[10] MA1_CS0-	MA1_CS0-	AC33	MA1_CS0_L
[10] MA1_CS1-	MA1_CS1-	AE34	MA1_CS1_L

MAAA17	AF33	MA_A0D17
MAAA16	AB34	MA_A0D16
MAAA15	AD32	MA_A0D15
MAAA14	AB35	MA_A0D14

[10] MA_ALERT-	MA_ALERT-	N34	MA_ALERT_L
[10] MA_PAROUT	MA_PAROUT	Y33	MA_PAROUT

MA_DATA[0]	E18	MDA0
MA_DATA[1]	J12	MDA1
MA_DATA[2]	J20	MDA2
MA_DATA[3]	H21	MDA3
MA_DATA[4]	H18	MDA4
MA_DATA[5]	F18	MDA5
MA_DATA[6]	G20	MDA6
MA_DATA[7]	F20	MDA7
MA_DATA[8]	H22	MDA8
MA_DATA[9]	G22	MDA9
MA_DATA[10]	E24	MDA10
MA_DATA[11]	J24	MDA11
MA_DATA[12]	F21	MDA12
MA_DATA[13]	J21	MDA13
MA_DATA[14]	H24	MDA14
MA_DATA[15]	F24	MDA15

MA_DATA[16]	J26	MDA16
MA_DATA[17]	J27	MDA17
MA_DATA[18]	G28	MDA18
MA_DATA[19]	H28	MDA19
MA_DATA[20]	G25	MDA20
MA_DATA[21]	C25	MDA21
MA_DATA[22]	E28	MDA22
MA_DATA[23]	H27	MDA23

MA_DATA[24]	F29	MDA24
MA_DATA[25]	J30	MDA25
MA_DATA[26]	H31	MDA26
MA_DATA[27]	F32	MDA27
MA_DATA[28]	J29	MDA28
MA_DATA[29]	G29	MDA29
MA_DATA[30]	E31	MDA30
MA_DATA[31]	G31	MDA31

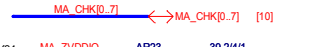
MA_DATA[32]	AJ34	MDA32
MA_DATA[33]	AJ30	MDA33
MA_DATA[34]	AK30	MDA34
MA_DATA[35]	AL34	MDA35
MA_DATA[36]	AH31	MDA36
MA_DATA[37]	AH32	MDA37
MA_DATA[38]	AK33	MDA38
MA_DATA[39]	AK32	MDA39

MA_DATA[40]	AM34	MDA40
MA_DATA[41]	AM33	MDA41
MA_DATA[42]	AP31	MDA42
MA_DATA[43]	AP33	MDA43
MA_DATA[44]	AL32	MDA44
MA_DATA[45]	AL31	MDA45
MA_DATA[46]	AP34	MDA46
MA_DATA[47]	AP32	MDA47

MA_DATA[48]	AF31	MDA48
MA_DATA[49]	AK29	MDA49
MA_DATA[50]	AM28	MDA50
MA_DATA[51]	AL28	MDA51
MA_DATA[52]	AM30	MDA52
MA_DATA[53]	AN30	MDA53
MA_DATA[54]	AP28	MDA54
MA_DATA[55]	AF28	MDA55

MA_DATA[56]	AK27	MDA56
MA_DATA[57]	AK26	MDA57
MA_DATA[58]	AP25	MDA58
MA_DATA[59]	AP25	MDA59
MA_DATA[60]	AN27	MDA60
MA_DATA[61]	AM27	MDA61
MA_DATA[62]	AL25	MDA62
MA_DATA[63]	AM25	MDA63

MA_CHECK[0]	F33	MA_CHK0
MA_CHECK[1]	G32	MA_CHK1
MA_CHECK[2]	K31	MA_CHK2
MA_CHECK[3]	K32	MA_CHK3
MA_CHECK[4]	E33	MA_CHK4
MA_CHECK[5]	E34	MA_CHK5
MA_CHECK[6]	J32	MA_CHK6
MA_CHECK[7]	J33	MA_CHK7



AM4B

MEMORY B

MAAB0	AC36	MB_A0C0[0]
MAAB1	U36	MB_A0C0[1]
MAAB2	U37	MB_A0C0[2]
MAAB3	T38	MB_A0C0[3]
MAAB4	T37	MB_A0C0[4]
MAAB5	R39	MB_A0C0[5]
MAAB6	R38	MB_A0C0[6]
MAAB7	P39	MB_A0C0[7]
MAAB8	R38	MB_A0C0[8]
MAAB9	P36	MB_A0C0[9]
MAAB10	AC39	MB_A0C0[10]
MAAB11	P37	MB_A0C0[11]
MAAB12	N38	MB_A0C0[12]
MAAB13	AC38	MB_A0C0[13]

[11] MB_ACT-	MB_ACT-	M38	MB_ACT_L
[11] MB_BG0	MB_BG0	M36	MB_BG0[0]
[11] MB_BG1	MB_BG1	M39	MB_BG1[0]

[11] MB_BA0	MB_BA0	AD38	MB_BA0[0]
[11] MB_BA1	MB_BA1	AC37	MB_BA1[0]

[11] MB_DM0[0.8]	MB_DM0	C21	MB_DM0[0]
	MB_DM1	D26	MB_DM1[0]
	MB_DM2	A32	MB_DM2[0]
	MB_DM3	D37	MB_DM3[0]
	MB_DM4	AL38	MB_DM4[0]
	MB_DM5	AF39	MB_DM5[0]
	MB_DM6	AT35	MB_DM6[0]
	MB_DM7	AW29	MB_DM7[0]
	MB_DM8	F39	MB_DM8[0]

DQSB0	B22	MB_DQSB[0]
DQSB1	A22	MB_DQSB[1]
DQSB2	C27	MB_DQSB[2]
DQSB3	B27	MB_DQSB[3]
DQSB4	C33	MB_DQSB[4]
DQSB5	C32	MB_DQSB[5]
DQSB6	B37	MB_DQSB[6]
DQSB7	A37	MB_DQSB[7]
DQSB8	AM37	MB_DQSB[8]
DQSB9	AM36	MB_DQSB[9]
DQSB10	AT38	MB_DQSB[10]
DQSB11	AT39	MB_DQSB[11]
DQSB12	AL34	MB_DQSB[12]
DQSB13	AV34	MB_DQSB[13]
DQSB14	AL28	MB_DQSB[14]
DQSB15	AL29	MB_DQSB[15]
DQSB16	C38	MB_DQSB[16]
DQSB17	G37	MB_DQSB[17]

U39	MB_CLK[0]
V39	MB_CLK[1]
W39	MB_CLK[2]
Y37	MB_CLK[3]
Y39	MB_CLK[4]
AA39	MB_CLK[5]

[11] MB_CLKH2	MB_CLKH2	Y37	MB_CLKH2[0]
[11] MB_CLKL2	MB_CLKL2	Y37	MB_CLKL2[0]
[11] MB_CLKH3	MB_CLKH3	Y39	MB_CLKH3[0]
[11] MB_CLKL3	MB_CLKL3	AA39	MB_CLKL3[0]

[11] MB_RST-	MB_RST-	K35	MB_RST_L
[11] MB_EVENT-	MB_EVENT-	AA38	MB_EVENT_L

[11] MB1_CKE0	MB1_CKE0	K37	MB1_CKE0[0]
[11] MB1_CKE1	MB1_CKE1	L36	MB1_CKE1[0]

[11] MODT_B2	MODT_B2	AF37	MB1_C0T0[0]
[11] MODT_B3	MODT_B3	AF38	MB1_C0T0[1]

[11] MB1_CS0-	MB1_CS0-	AE37	MB1_CS0_L
[11] MB1_CS1-	MB1_CS1-	AG36	MB1_CS1_L

MAAB17	AH37	MB_A0D17
MAAB16	AD36	MB_A0D16
MAAB15	AF36	MB_A0D15
MAAB14	AD39	MB_A0D14

[11] MB_ALERT-	MB_ALERT-	N37	MB_ALERT_L
[11] MB_PAROUT	MB_PAROUT	AR38	MB_PAROUT

MB_DATA[0]	D20	MOB0
MB_DATA[1]	B21	MOB1
MB_DATA[2]	B24	MOB2
MB_DATA[3]	C24	MOB3
MB_DATA[4]	A20	MOB4
MB_DATA[5]	A23	MOB5
MB_DATA[6]	A23	MOB6
MB_DATA[7]	C23	MOB7

MB_DATA[8]	A26	MOB8
MB_DATA[9]	C26	MOB9
MB_DATA[10]	A29	MOB10
MB_DATA[11]	C29	MOB11
MB_DATA[12]	A25	MOB12
MB_DATA[13]	B25	MOB13
MB_DATA[14]	A28	MOB14
MB_DATA[15]	B28	MOB15

MB_DATA[16]	A31	MOB16
MB_DATA[17]	B31	MOB17
MB_DATA[18]	B34	MOB18
MB_DATA[19]	C35	MOB19
MB_DATA[20]	B30	MOB20
MB_DATA[21]	C30	MOB21
MB_DATA[22]	B33	MOB22
MB_DATA[23]	A34	MOB23

MB_DATA[24]	B36	MOB24
MB_DATA[25]	E36	MOB25
MB_DATA[26]	C39	MOB26
MB_DATA[27]	D38	MOB27
MB_DATA[28]	A35	MOB28
MB_DATA[29]	C36	MOB29
MB_DATA[30]	B38	MOB30
MB_DATA[31]	C38	MOB31

MB_DATA[32]	AK39	MOB32
MB_DATA[33]	AL37	MOB33
MB_DATA[34]	AN36	MOB34
MB_DATA[35]	AN39	MOB35
MB_DATA[36]	AK38	MOB36
MB_DATA[37]	AK36	MOB37
MB_DATA[38]	AM39	MOB38
MB_DATA[39]	AN38	MOB39

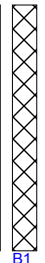
MB_DATA[40]	AF36	MOB40
MB_DATA[41]	AF37	MOB41
MB_DATA[42]	AL37	MOB42
MB_DATA[43]	AF37	MOB43
MB_DATA[44]	AF37	MOB44
MB_DATA[45]	AP38	MOB45
MB_DATA[46]	AT36	MOB46
MB_DATA[47]	AL38	MOB47

MB_DATA[48]	AW35	MOB48
MB_DATA[49]	AL35	MOB49
MB_DATA[50]	AW32	MOB50
MB_DATA[51]	AL32	MOB51
MB_DATA[52]	AW36	MOB52
MB_DATA[53]	AW36	MOB53
MB_DATA[54]	AW33	MOB54
MB_DATA[55]	AW33	MOB55

MB_DATA[56]	AW30	MOB56
MB_DATA[57]	AW30	MOB57
MB_DATA[58]	AW27	MOB58
MB_DATA[59]	AW26	MOB59
MB_DATA[60]	AW31	MOB60
MB_DATA[61]	AL31	MOB61
MB_DATA[62]	AW28	MOB62
MB_DATA[63]	AW27	MOB63

MB_CHECK[0]	F38	MB_CHK0
MB_CHECK[1]	E36	MB_CHK1
MB_CHECK[2]	H39	MB_CHK2
MB_CHECK[3]	J39	MB_CHK3
MB_CHECK[4]	E37	MB_CHK4
MB_CHECK[5]	E39	MB_CHK5
MB_CHECK[6]	H36	MB_CHK6
MB_CHECK[7]	H37	MB_CHK7

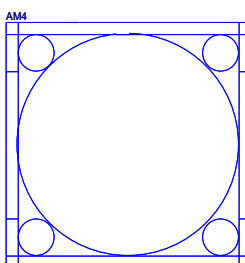
MEM CHB

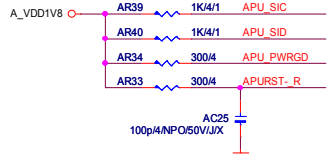


MEM CHA

CPU SOCKET : G-FL

[10] MDA[0.63]	MDA[0.63]
[10] MAAA[0.17]	MAAA[0.17]
[10] DQSA[0.8]	DQSA[0.8]
[10] -DQSA[0.8]	-DQSA[0.8]



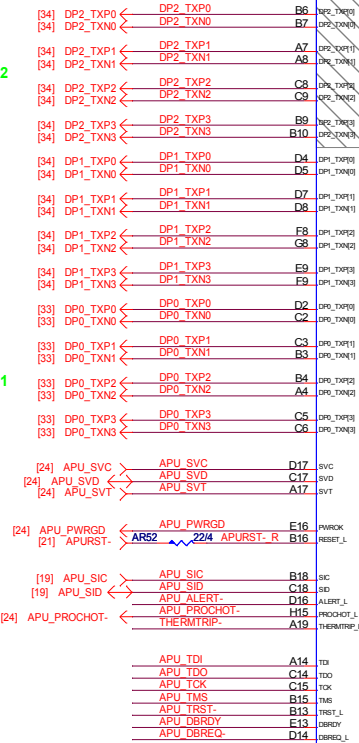


SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

HDMI2

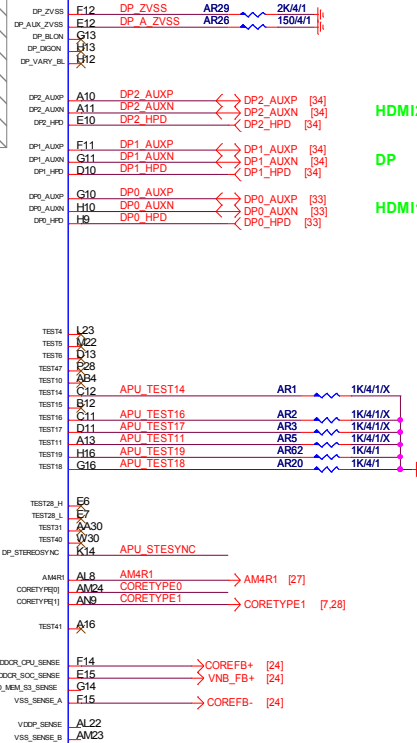
DP

HDMI1



AMC
CPU-SK/1331BK/S/GF/10SC1-P01331-21R_10SC1-P01331-23R

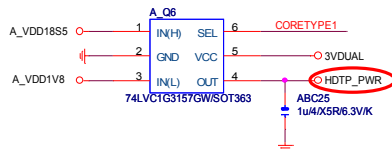
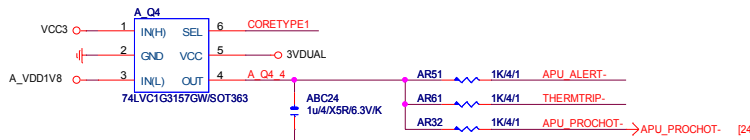
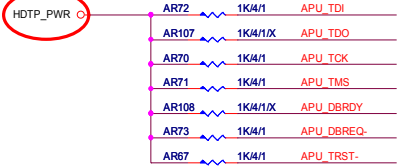
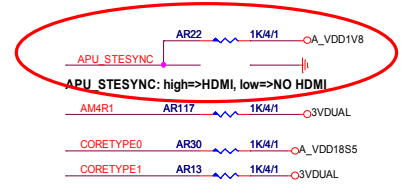
Placed within 1500 mils from APU



HDMI2

DP

HDMI1

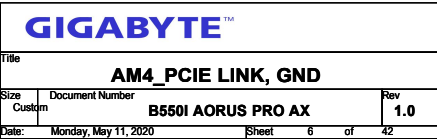


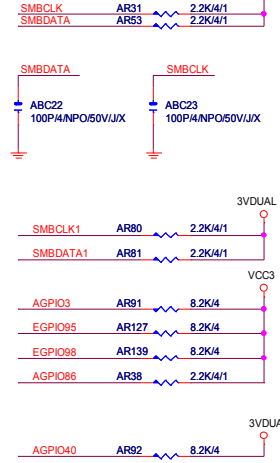
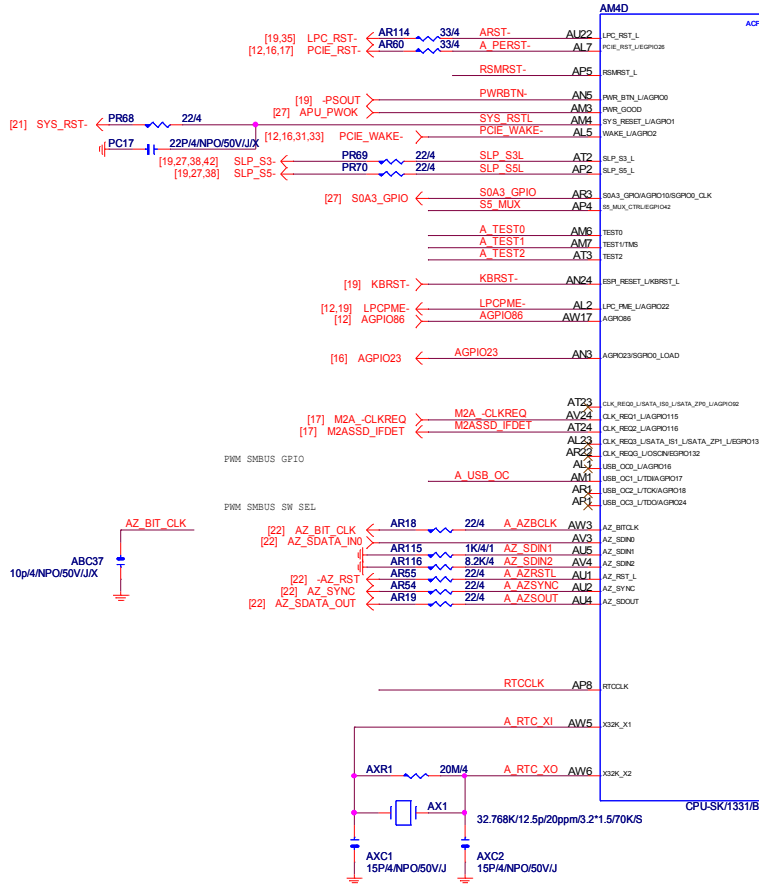
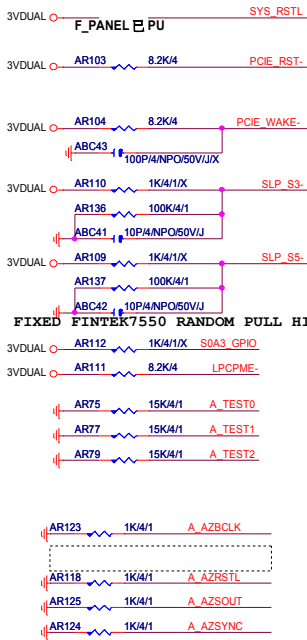
AM4 CPU CoreType

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15h, 60 h- 6 Fh	TYPE 0
0	1		TYPE 1
1 ST	0	Family 17h, Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17h, Models 10 h- 1 Fh Family 17h, Models 20h-2Fh	TYPE 3

GIGABYTE™

Title	CPU CONTROL	
Size	Document Number	Rev
Custom	B550I AORUS PRO AX	1.0
Date:	Monday, May 11, 2020	Sheet 5 of 42

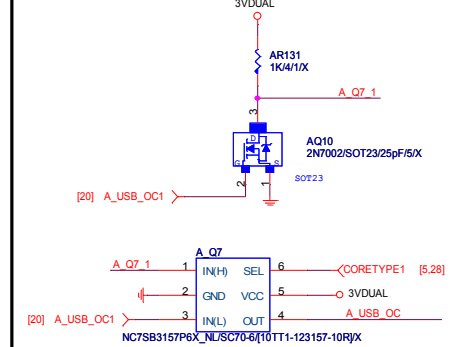




For AMD X570 NO EC WATCH DOG.

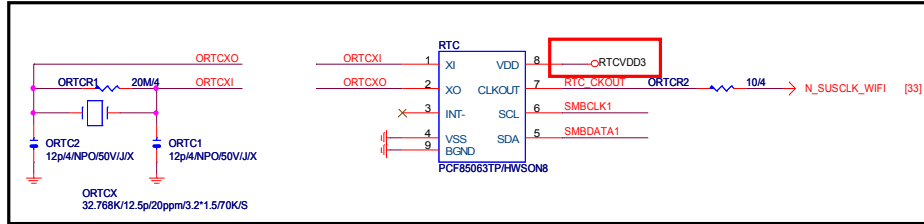


For AMD NO EC USB OC.



Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



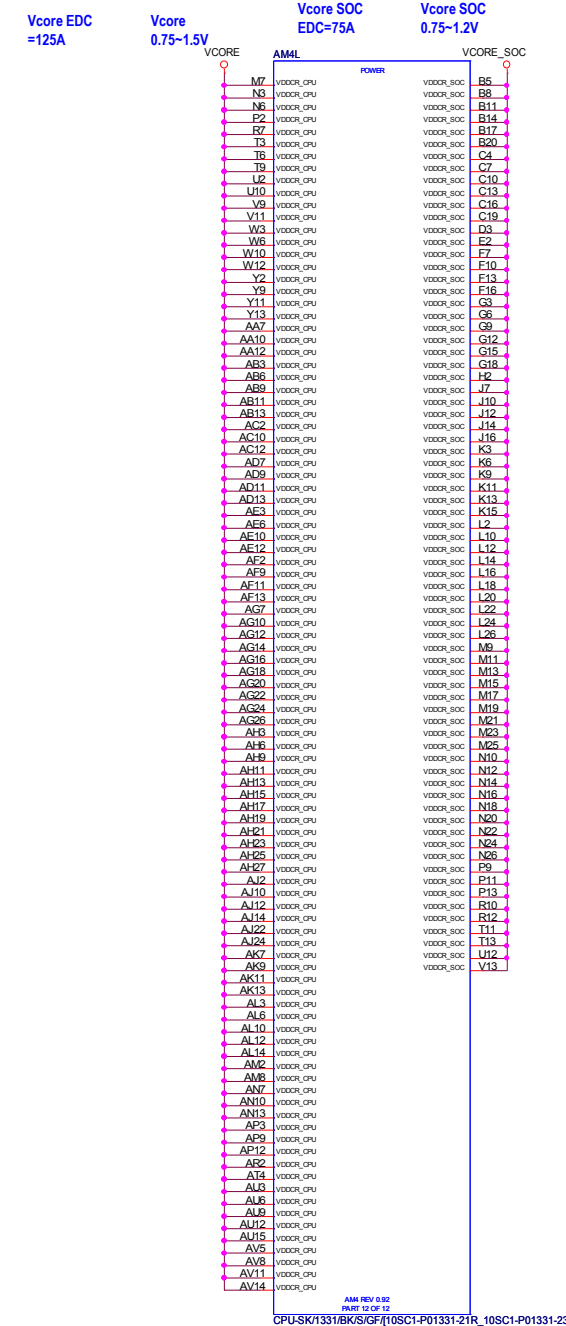
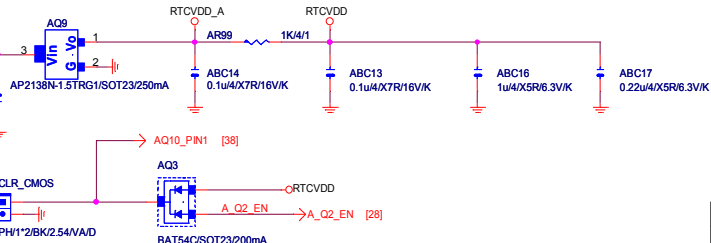
GIGABYTE™

Title	AM4 MISC	Rev	1.0
Size	Document Number	B550I AORUS PRO AX	
Custom	Date	Monday, May 11, 2020	Sheet 7 of 42

AM4 1.5V, 250mA (A_V15S5)
A_Q1 改接A_VDD18S5 for VDDIO_AUDIO


For STR FAIL ISSUE

VDDCR_SOC_S5 -->N/A

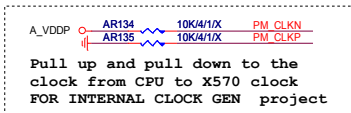


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

			
Title <div style="text-align: center;">CPU POWER & GND</div>			
Size Custom	Document Number <div style="text-align: center;">B550I AORUS PRO AX</div>		Rev <div style="text-align: center;">1.0</div>
Date Monday, May 11, 2020	Sheet 8 of 42		

	SPI_CLK	LFRAME	SYS_RST	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.



[16] A_GFX_CLKP ←

[16] A_GFX_CLKN ←

```
[17] M2A_CLKP  >
[17] M2A_CLKN  >
```

[12] PM_CLKP 

[12] PM_CLKN

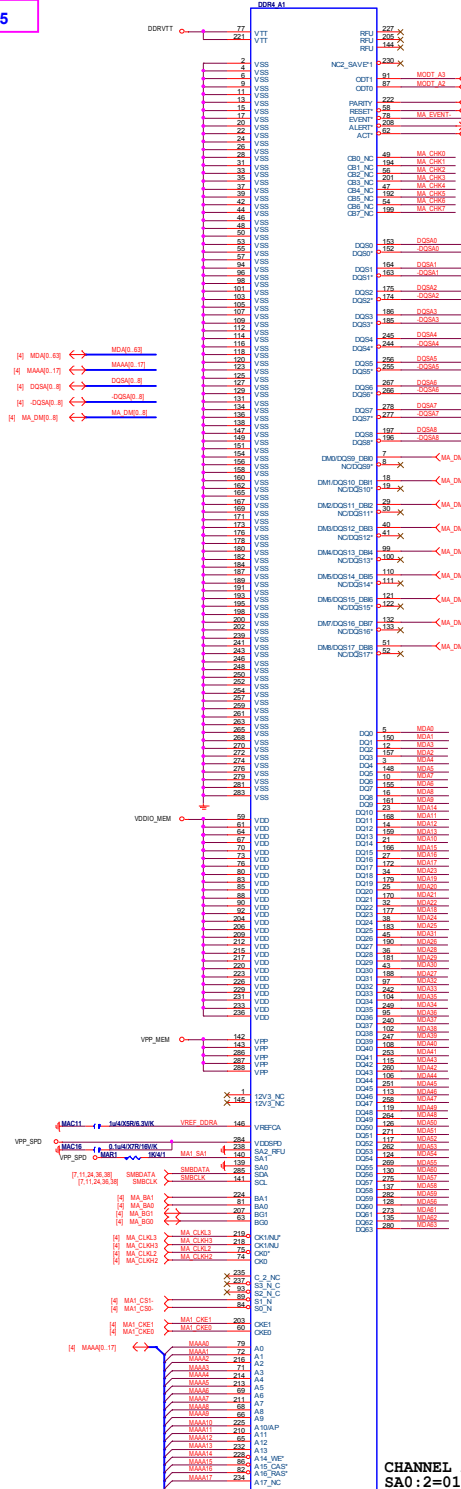


A_VDD1V8



256Mb VALUE: 256M/WS0N8/200MIL/S



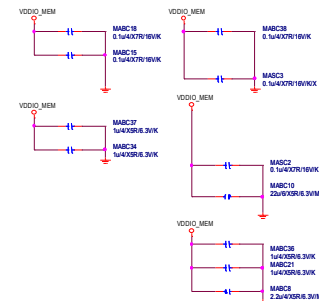


CHANNEL A0
SA0:2=010

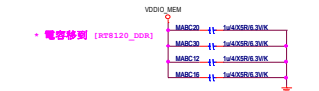
DOR4288/BK/VA/D/GF/TWO LATCH/SHELL/C7025/11SM1-521288-G1
BLACK

* 金屬加強黑色slot

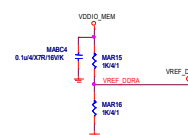
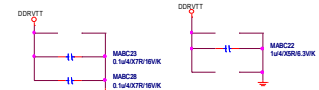
DDR12V Decouple

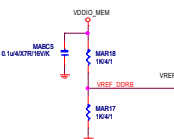


* 電容移到 [RT8120_DDR]



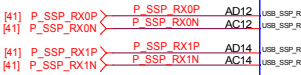
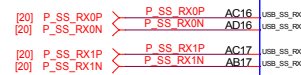
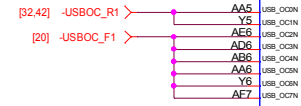
DDRVTT Decouple





BLACK

USB port power control 9:0
(VCC3). Output.



USB Controller 0: USB20 [0:5], USB30 [0:3]
USB Controller 1: USB20 [6:11], USB30 [4:7]

USB30G2	USB20
0	4
1	4
2	5
3	5
4	9
5	8
6	7
7	6

USB30_I211 Lan

F_USB 30_2

F_USB 30_1

FRONT TYPE C

HSD 10

HSD 11

HSD 6

HSD 7

HSD 8

HSD 9

HSD 5

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7

R_TYPE A

R_TYPE C

F_USB30

F_USB20

MCU(IT5702)

M2_WIFI

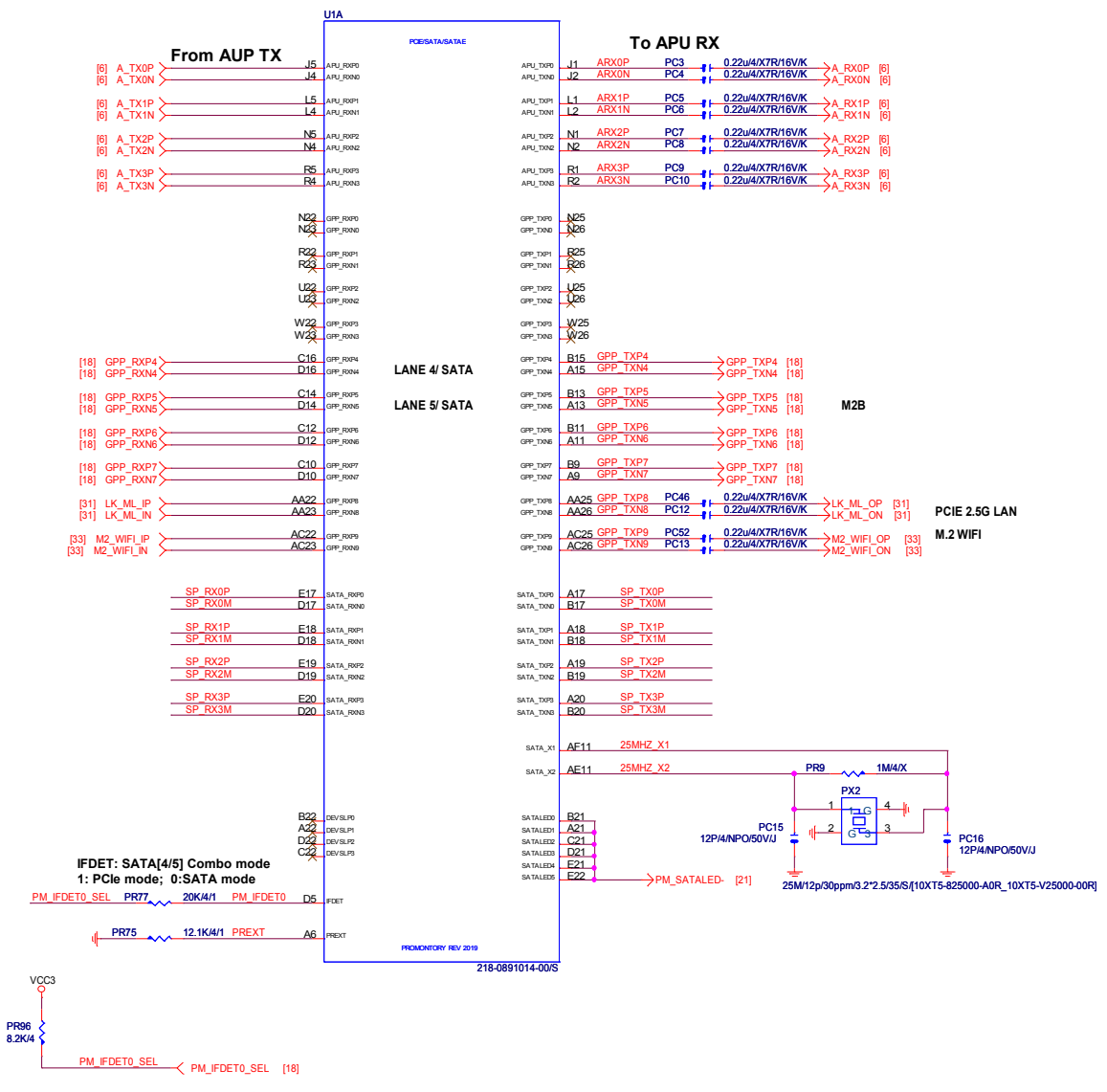
F_USB30

R_TYPE A

R_TYPE C

GIGABYTE™ ANIS 7868376

Title			PM USB
Size	Document Number	Rev	
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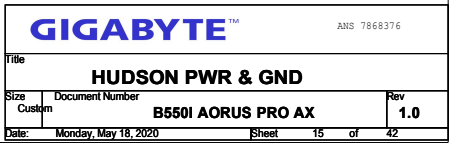
注意 PIN DEFINE.

SATA3_1

SATA3_2

注意 PIN DEFINE.

SATA3_3



PCIE M.2 Plug-in : L

DATA : GND. PCIE : NC

架高,金屬殼,正面
8.5H鐵殼M.2 M key for Gen4.0.料號:
10NR5-130M67-51R
NEW FOOTPRINT: M2_80_CUT42

DIP螺絲 (TOP)

DIP螺柱 (TOP)

SMD螺柱(TOP)

M.2 Level Shift for M.2 & PCIE slot的SMBus,可控RGB M.2/AIC SSD.

GIGABYTE™

Title: M.2 SOCKET

Size: B550I AORUS PRO AX

Document Number: 1.0

Date: Monday, May 11, 2020

Sheet 17 of 42

[illegible]

PCIE M.2 Plug-in : L

DATA : GND. PCIE : NC

架高,金屬殼,正面
8.5H鐵殼M.2 M key for Gen4.0.料號:
10NR5-130M67-51R
NEW FOOTPRINT: M2_80_CUT42

DIP螺絲 (TOP)

DIP螺柱 (TOP)

SMD螺柱(TOP)

M.2 Level Shift for M.2 & PCIE slot的SMBus,可控RGB M.2/AIC SSD.

GIGABYTE™

Title: M.2 SOCKET

Size: B550I AORUS PRO AX

Document Number: 1.0

Date: Monday, May 11, 2020

Sheet 17 of 42

[illegible]

PCIE M.2 Plug-in : L

DATA : GND. PCIE : NC

架高,金屬殼,正面
8.5H鐵殼M.2 M key for Gen4.0.料號:
10NR5-130M67-51R
NEW FOOTPRINT: M2_80_CUT42

DIP螺絲 (TOP)

DIP螺柱 (TOP)

SMD螺柱(TOP)

M.2 Level Shift for M.2 & PCIE slot的SMBus,可控RGB M.2/AIC SSD.

GIGABYTE™

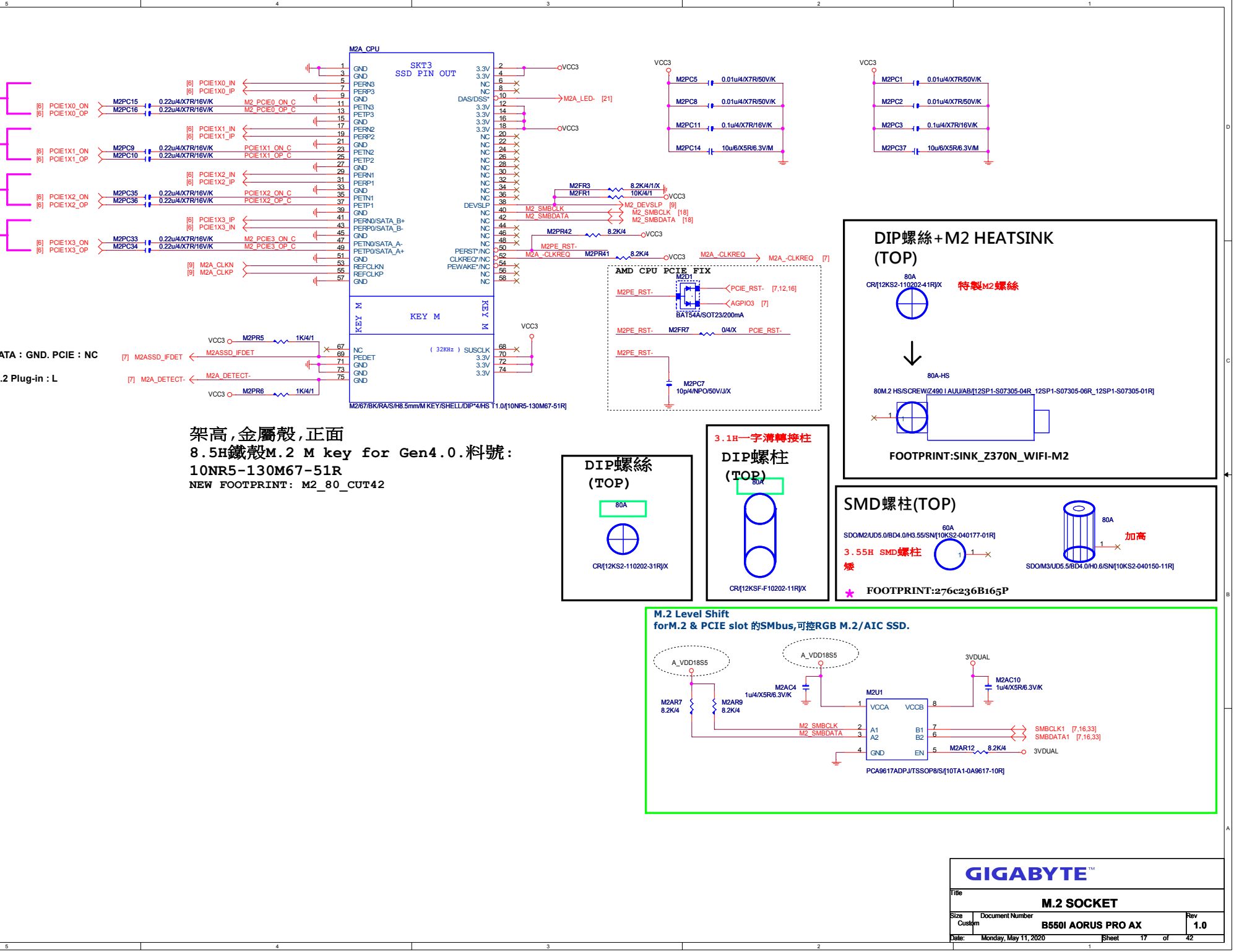
Title: M.2 SOCKET

Size: B550I AORUS PRO AX

Document Number: 1.0

Date: Monday, May 11, 2020

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SATA : GND. PCIE : NC

.2 Plug-in : L

架高,金屬殼,正面 8.5H鐵殼M.2 M key for Gen4.0.料號: 10NR5-130M67-51R NEW FOOTPRINT: M2_80_CUT42

DIP螺絲+M2 HEATSINK (TOP)

特製M2螺絲

↓

80A-HS

80M 2 HS/SCREW/Z490 I AUU/AB[12SP1-S07305-04R 12SP1-S07305-06R 12SP1-S07305-01R]

FOOTPRINT:SINK_Z370N_WIFI-M2

DIP螺柱 (TOP)

加高

SDOM3UD5.0BD4.0H3.55/SIN[10KS2-040177-01R]

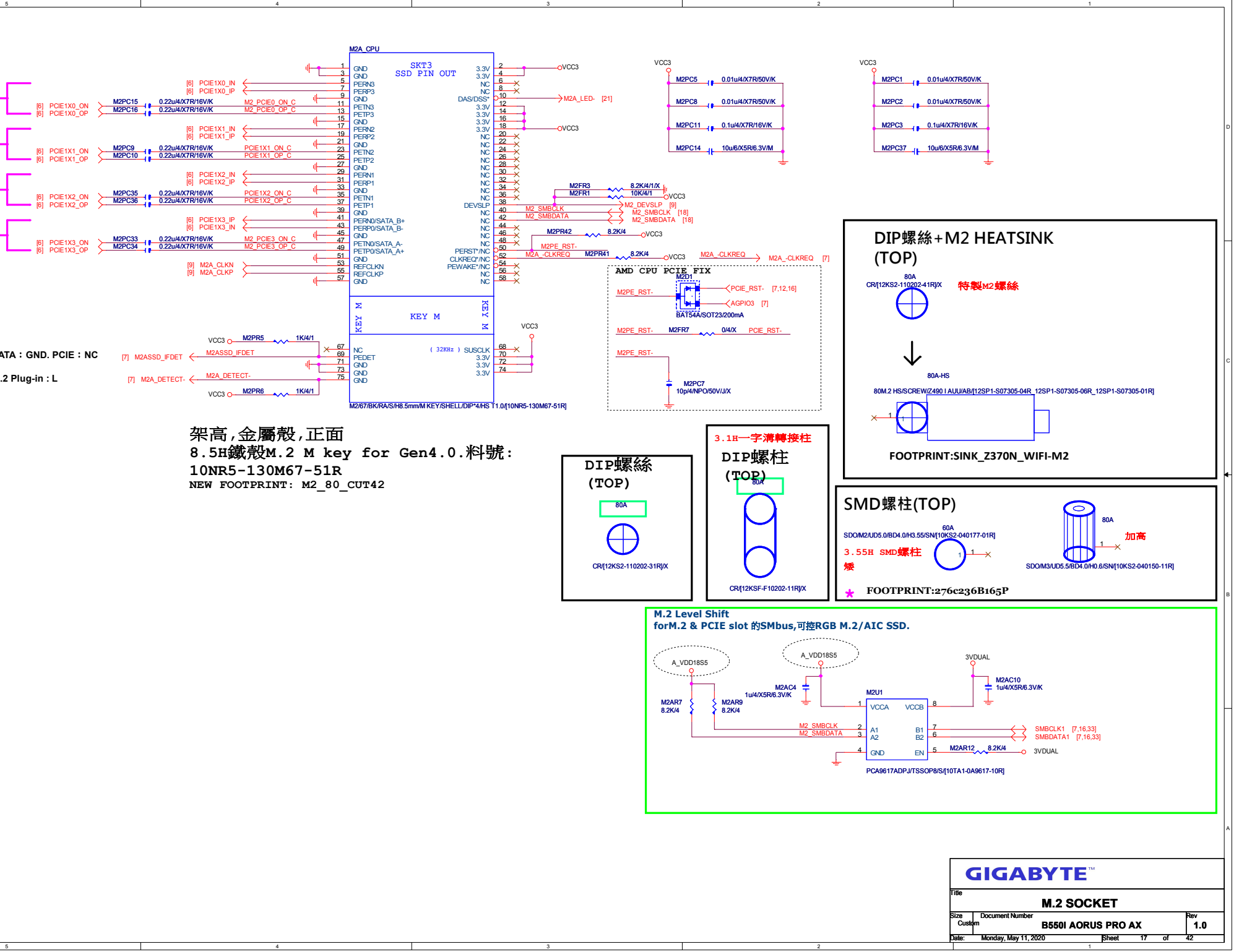
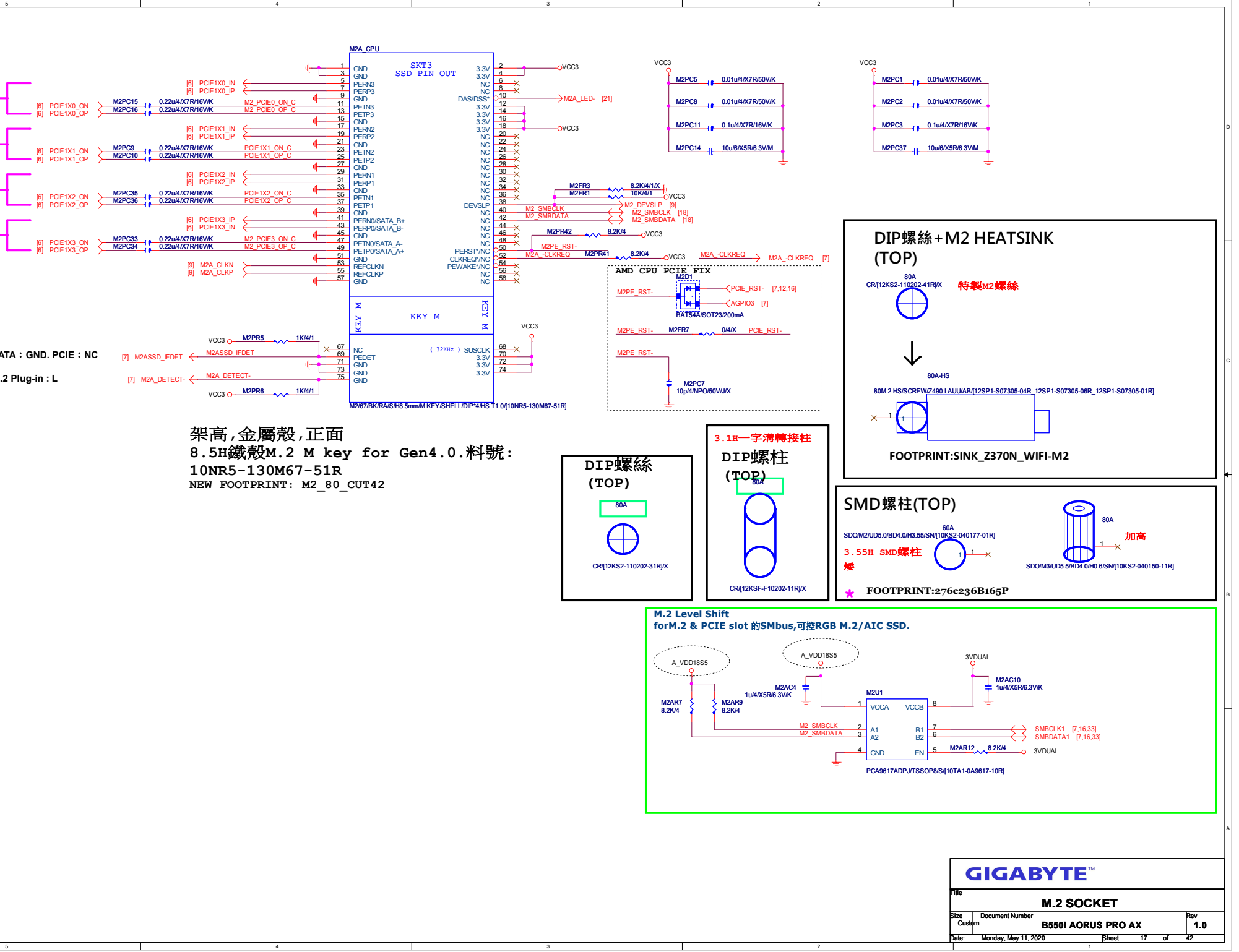
* FOOTPRINT:276c236B165P

M.2 Level Shift for M.2 & PCIe slot的SMBus,可控RGB M.2/AIC SSD.

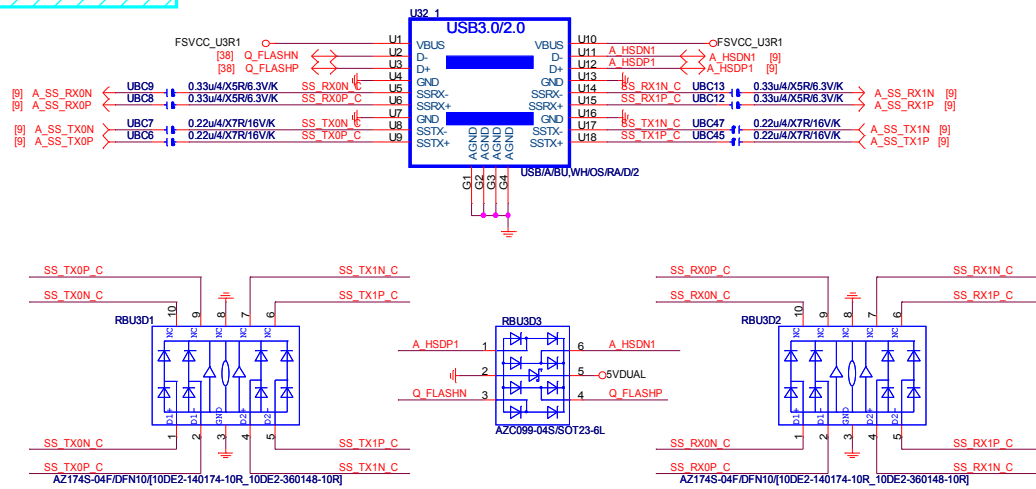
```

graph LR
    VDD1[VCC] --- R1[M2AR7 8.2KΩ] --- J1(( ))
    J1 --- R2[M2AR9 8.2KΩ] --- P1[PIN 1]
    J1 --- R3[M2AC4 1μF/X5R6.3V/K] --- P1
    
    VDD2[VCC] --- R4[M2AR7 8.2KΩ] --- J2(( ))
    J2 --- R5[M2AR9 8.2KΩ] --- P2[PIN 2]
    J2 --- R6[M2AC4 1μF/X5R6.3V/K] --- P2
    
    P1 -- "M2 SMBCLK [7.16.33]" --- P3[PIN 7]
    P2 -- "M2 SMBDATA [7.16.33]" --- P4[PIN 8]
    
    EN[PIN 5] --- R7[M2AR12 8.2KΩ] --- VDDUAL[VCC]
  
```

GIGABYTE™		
Title	M.2 SOCKET	
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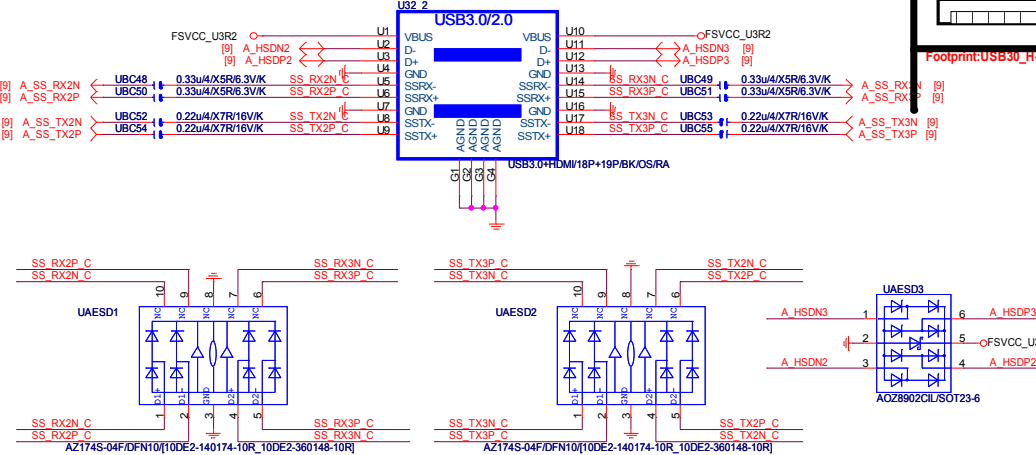
[illegible]

FROM CPU WITH Q_FALSH



R_USB30_HDMI

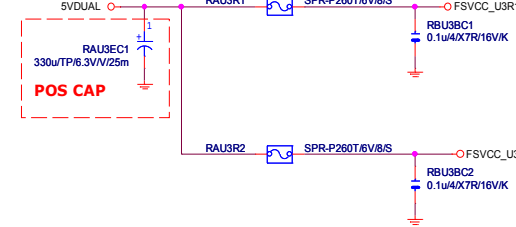
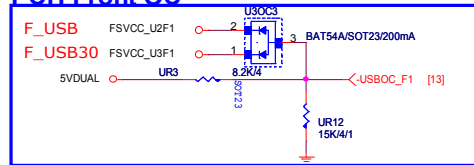
FROM CPU



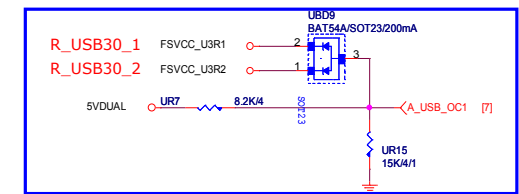
PCH REAR OC



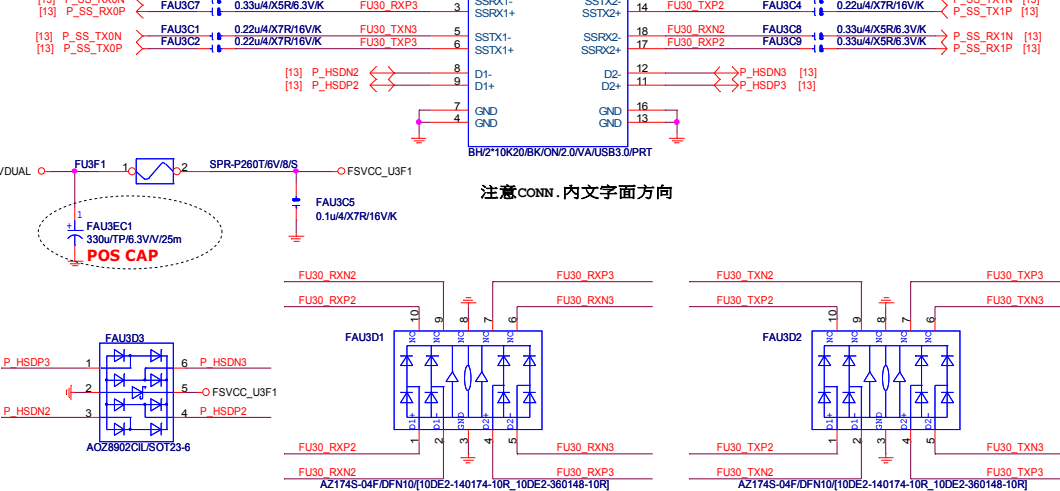
PCH Front OC



CPU REAR OC

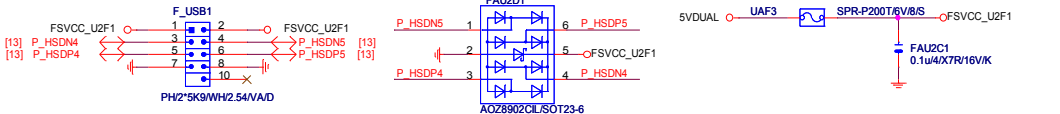


FROM PCH



FRONT SIDE USB1

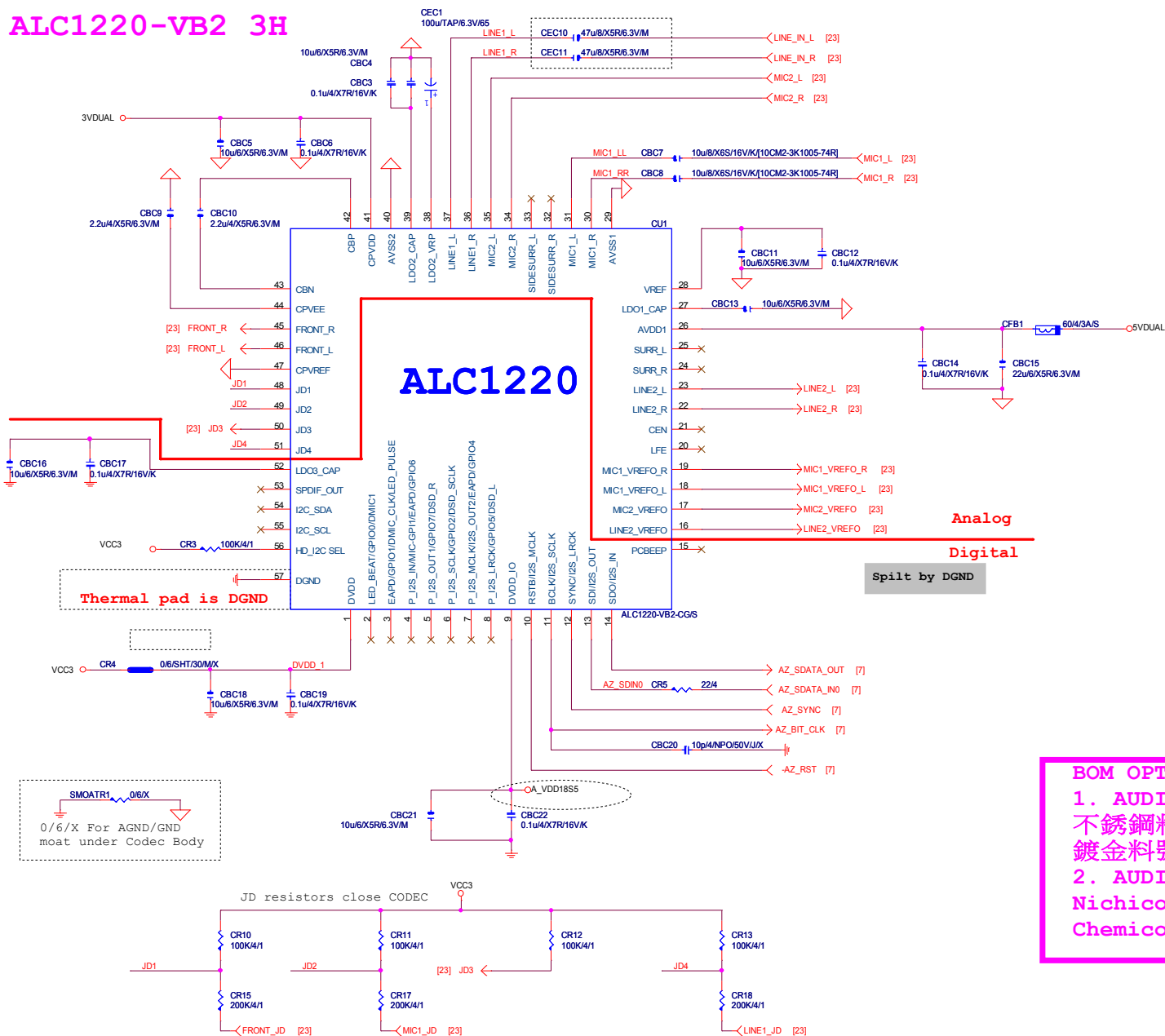
FROM PCH



Rev 4.1

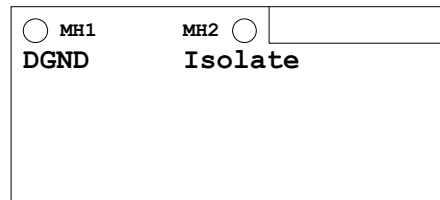
ALC1220-VB2 3H

FOOTPRINT: C0805-L-1



LAYOUT注意: 螺絲孔下GND方式

1. MH1下DGND
2. MH2一律改為Isolate



LAYOUT注意: 是否要加?

AGND切割線



Analog

Digital

Spilt by DGND

BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號: 11NR6-403025-A3R

鍍金料號: 11NR6-403025-92R

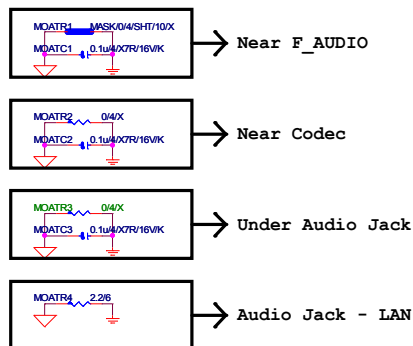

2. AUDIO CAP

Nichicon MW音效電容 : 100u/TAP/6.3V/65

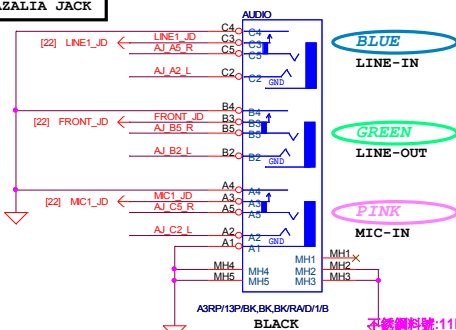
Chemicon音效電容 : 100uF/TAP/10V/6*5

GIGABYTE

Title			
ALC1220 CODEC			
Size	Document Number	Rev	
Custom	B550I AORUS PRO AX	1.0	
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AZALIA JACK



不銹鋼料號:11NR6-403025-A3R
鍍金料號:11NR6-403025-92R

[22] FRONT_R ← CR20 754/1 AJ B5_R

[22] FRONT_L ← CR21 754/1 AJ B2_L

CD3 AZZZ5-01U/S00323

CD4 AZZZ5-01U/S00323

CBC25 180p4/NPO/50VJ

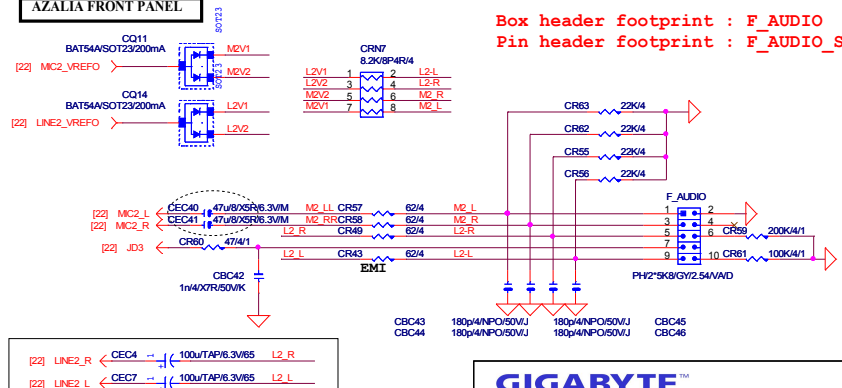
CBC26 180p4/NPO/50VJ

[illegible]

The schematic diagram illustrates the power supply section of the BATS44AS/SOT23-200mA. It features a 624V input connected to a network of resistors (CR25, CR28, CR142, CR143) and capacitors (CQ13, CR29, CR30). The output is connected to the MC1_R, MC1_L, and MC1_VREF0_L pins. The input is also connected to the AI_CS_R and AI_C2_L pins. The input is also connected to the AI_CS_R and AI_C2_L pins.

CEN/LFE

AZALIA FRONT PANEL

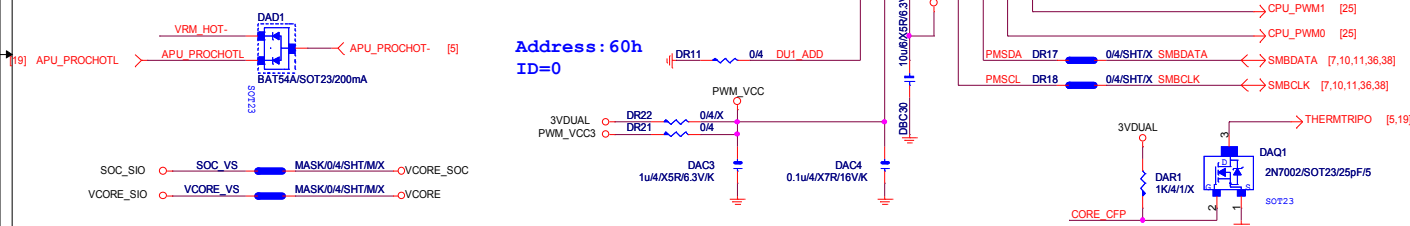
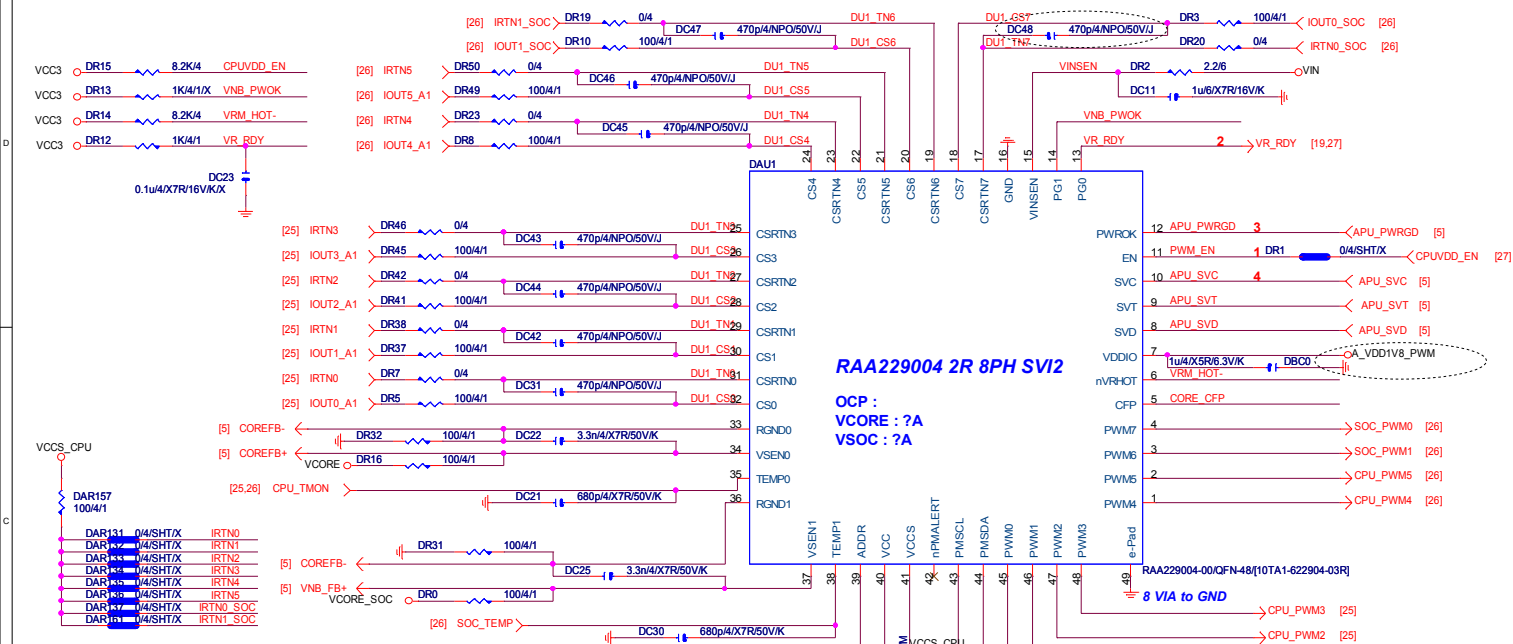


```
Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO S
```

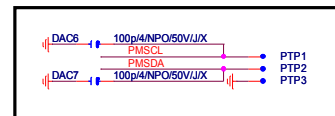
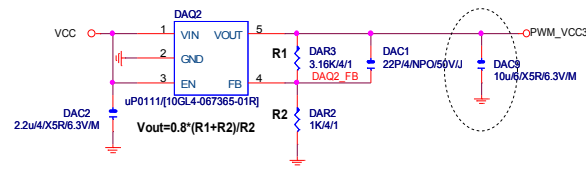
GIGABYTE™

Title			
AUDIO JACK			
Size	Document Number		Rev
Custom	B5501 AORUS PRO AX		1.0
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REV:0.11

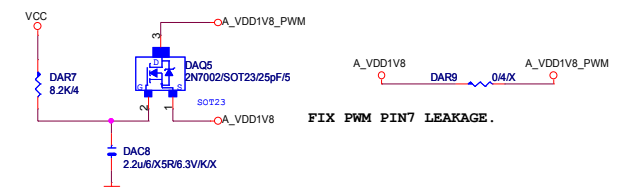
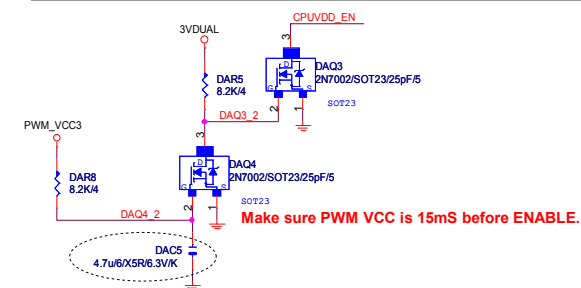
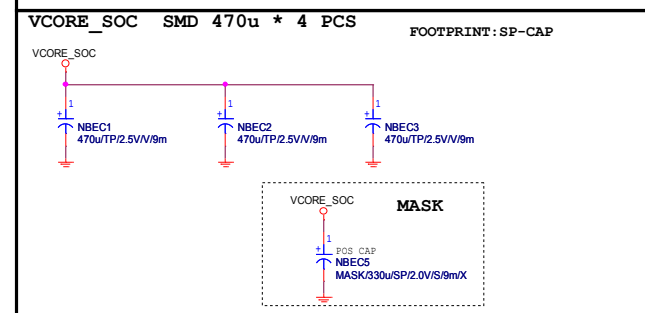
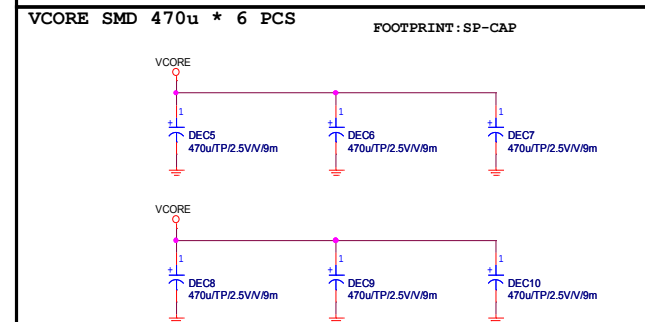
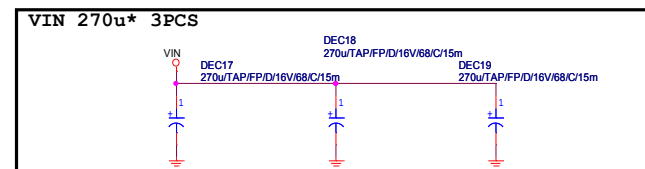
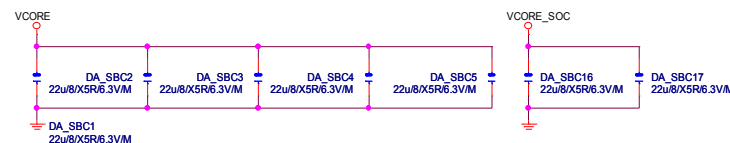


SiC651ACD-T1-GE3/MLP55-31L 3.3V PWM 651ACD
SiC651CD-T1-GE3/MLP55-31L 5V PWM 651CD
RAA229004 X+Y=8, 3.3V PWM
1SL6617A 5V PWM DOUBLER
RAA229004 3.3V PWM + 651ACD
RAA229004 3.3V PWM + 6617A + 651CD

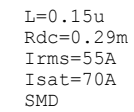


放置背板電感與電感之間

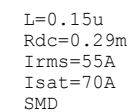
放置背板電感與電感之間



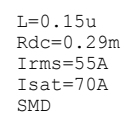
10u/8/X6S/16V/K
10u/8/X6S/16V/K



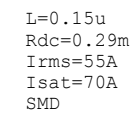
10u/8/X6S/16V/K
10u/8/X6S/16V/K



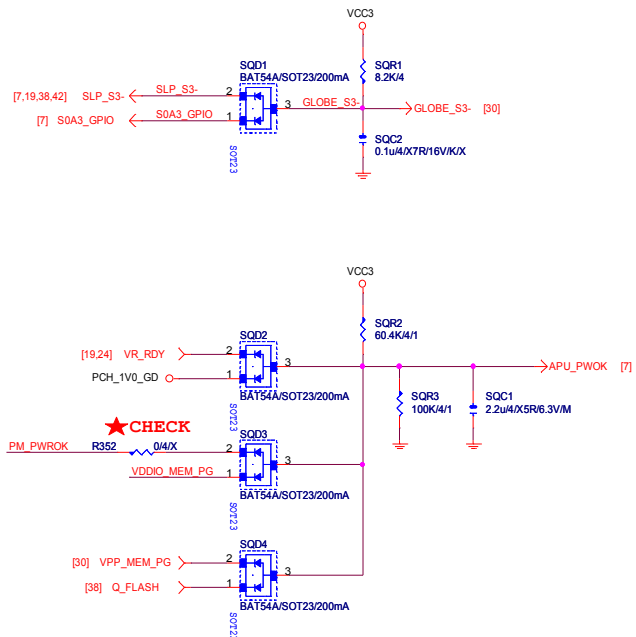
10u/8/X6S/16V/K
10u/8/X6S/16V/K



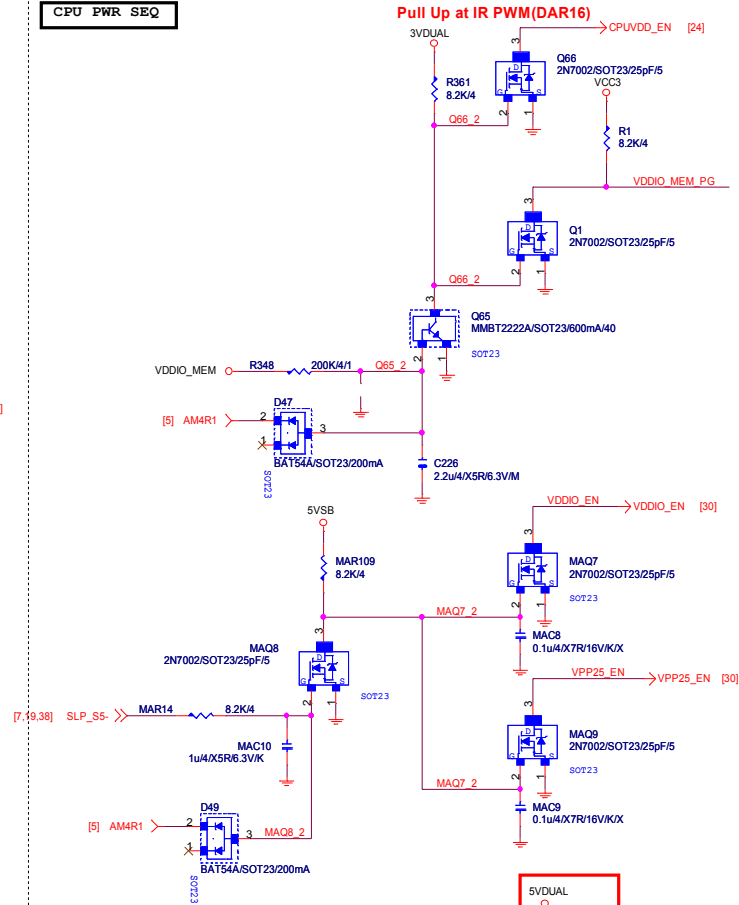
10u/8/X6S/16V/K
10u/8/X6S/16V/K



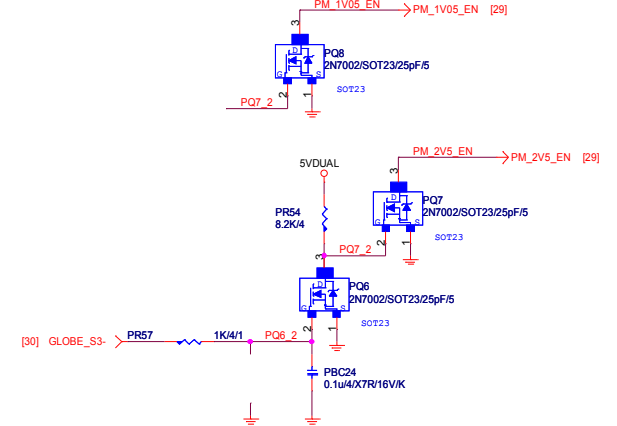
PWR SEQ



CPU	PWR	SEQ
-----	-----	-----

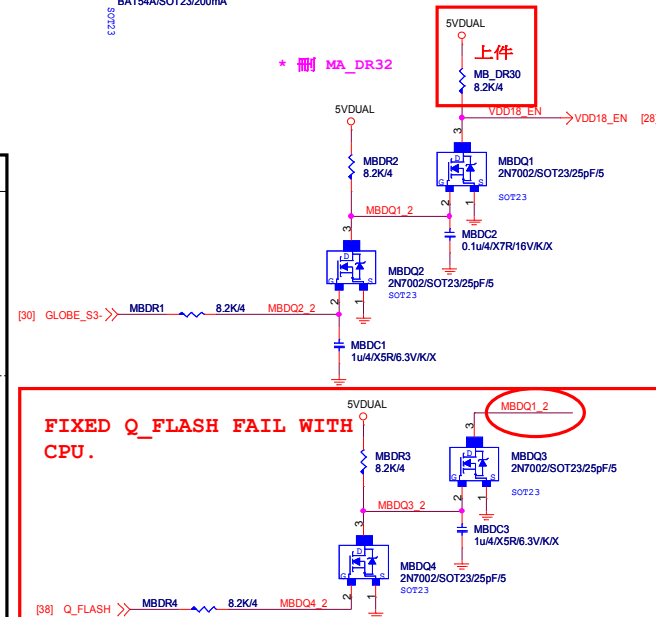


PM SWR SEQ

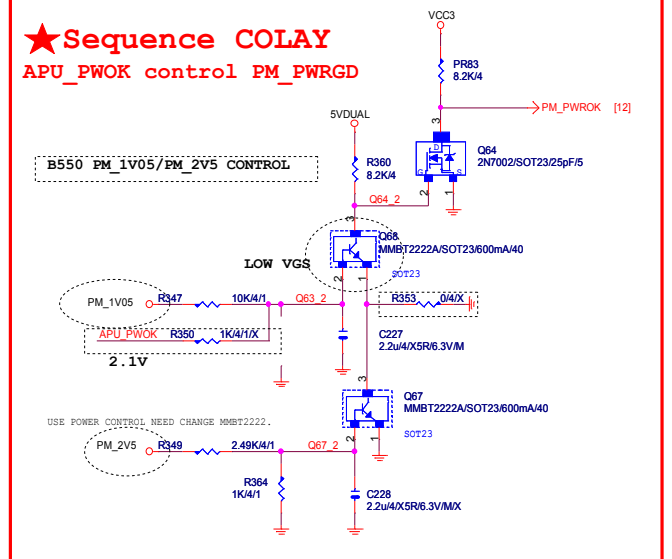


B550 I AORUS PRO WIFI POWER RAIL DESING

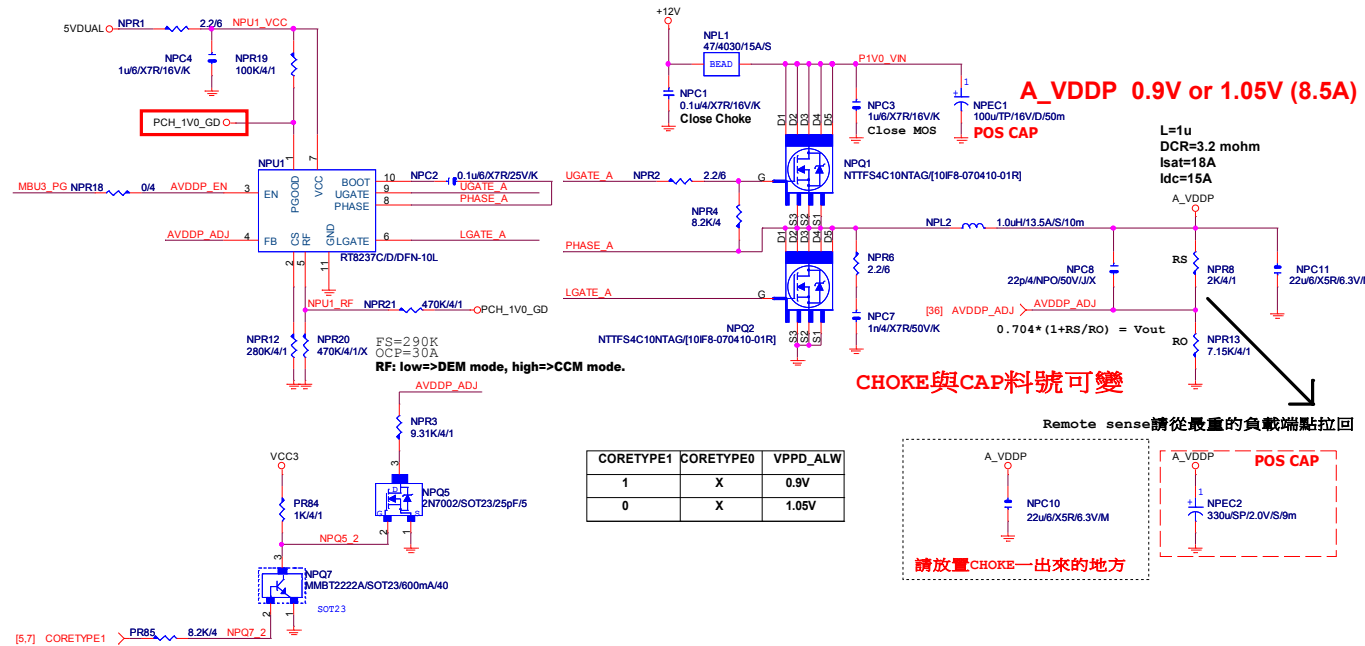
	CPU POWER RAIL	B550 POWER RAIL
S5 POWER		
S0 POWER		



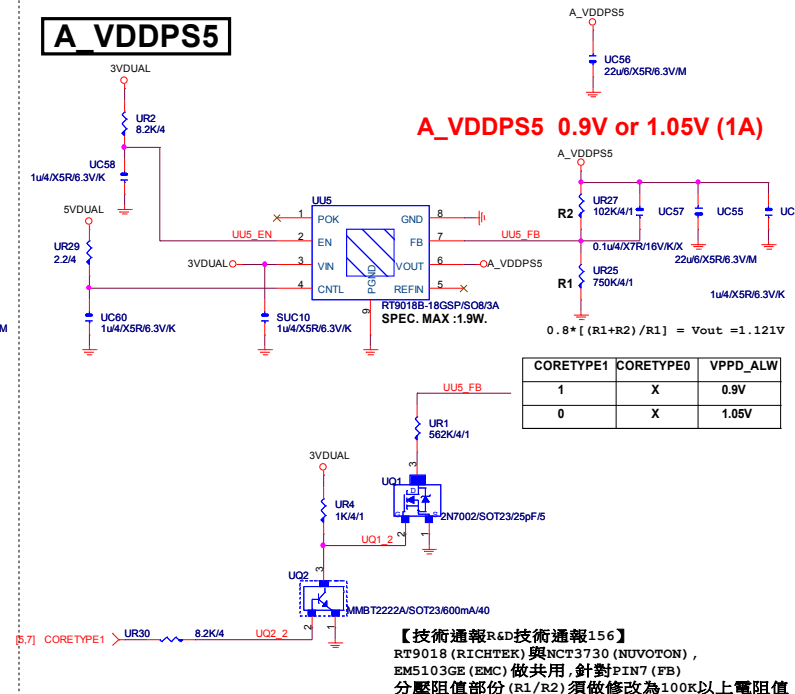
★ Sequence COLAY
APU PWOK control PM PWRGD



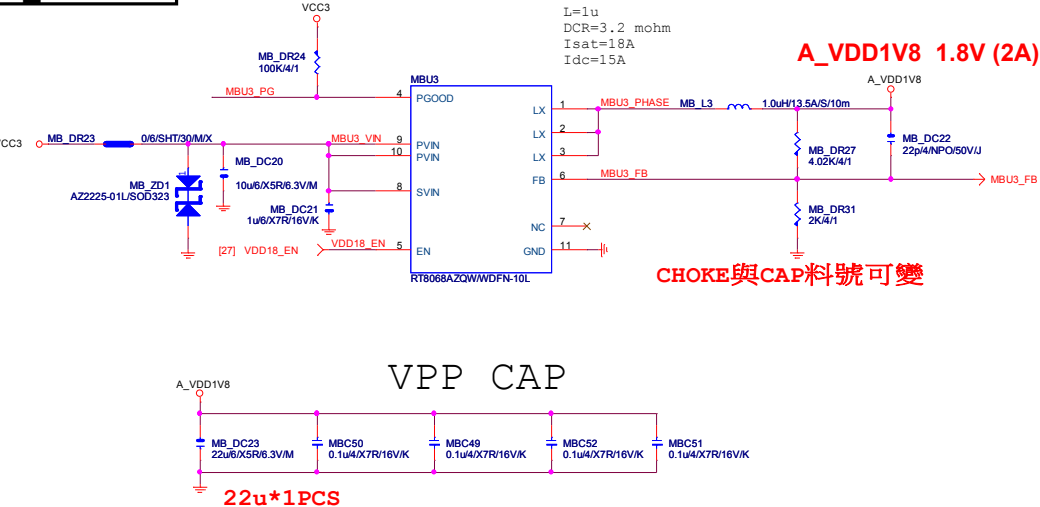
A_VDDP



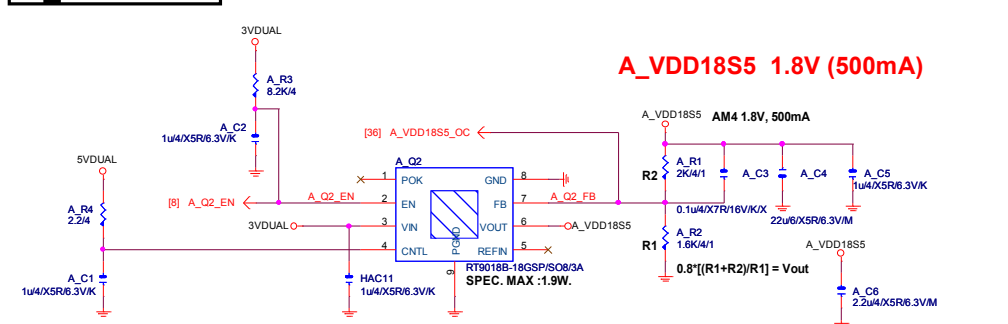
A_VDDPS5



A_VDD1V8



A_VDD18S5



VDDCR SOC S5

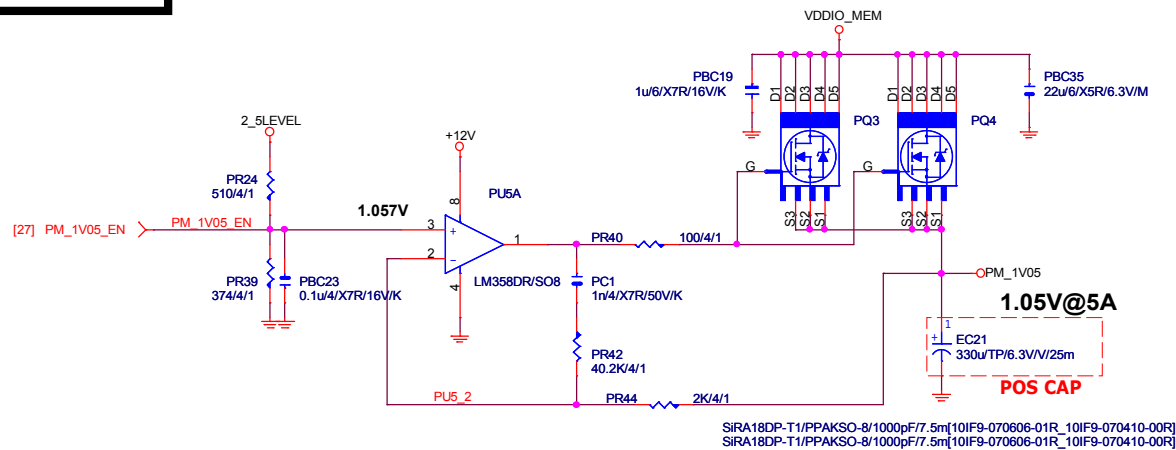
N/A

S5_MUX: S0->High, S5->Low

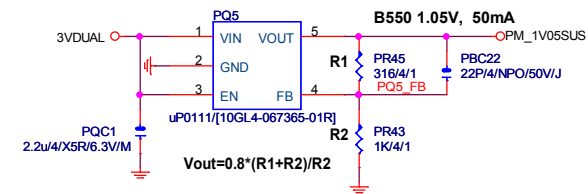
H: VDDCR_SOC_S5 will track VCORE_SOC.

L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will trace VCORE_SOC.

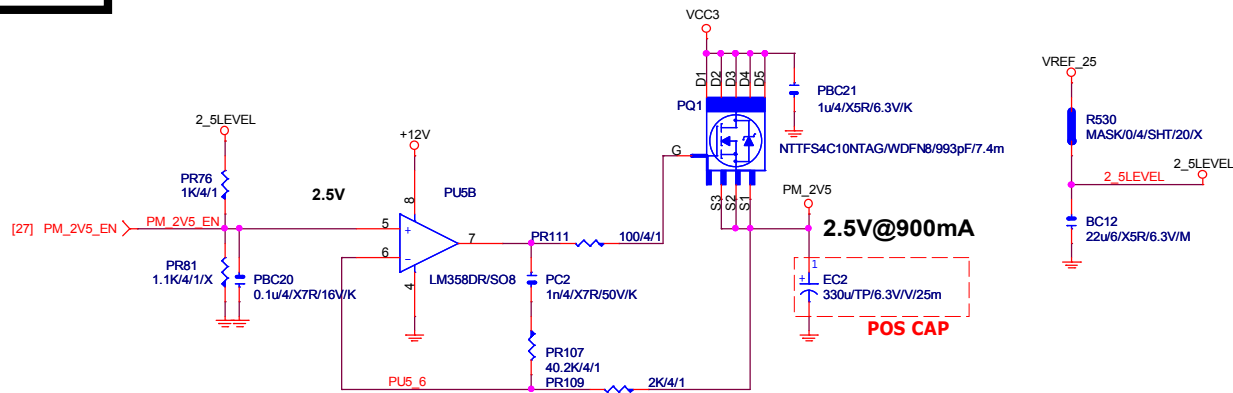
PM_1V05



PM_1V05SUS



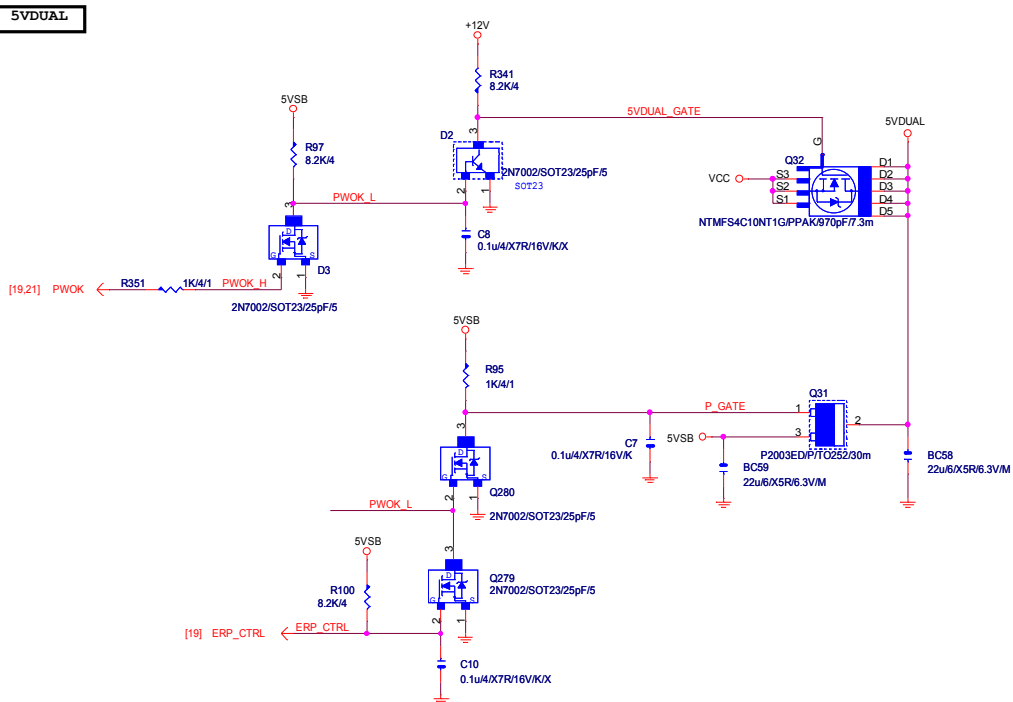
PM_2V5



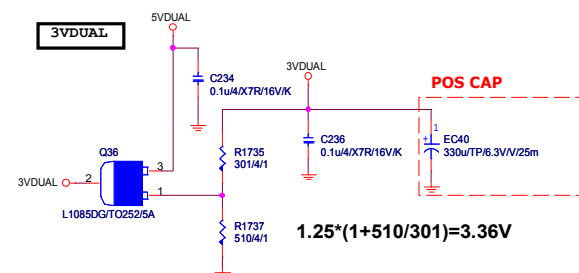
GIGABYTE™

Title			PM POWER
Size B	Document Number	B550I AORUS PRO AX	
Date: Monday, May 11, 2020		Sheet 29	of 42
		Rev 1.0	

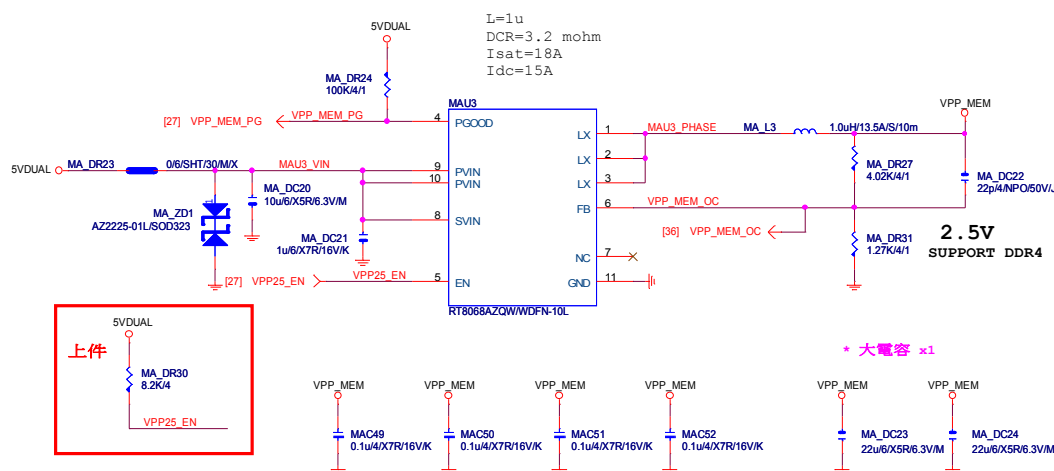
5VDUAL



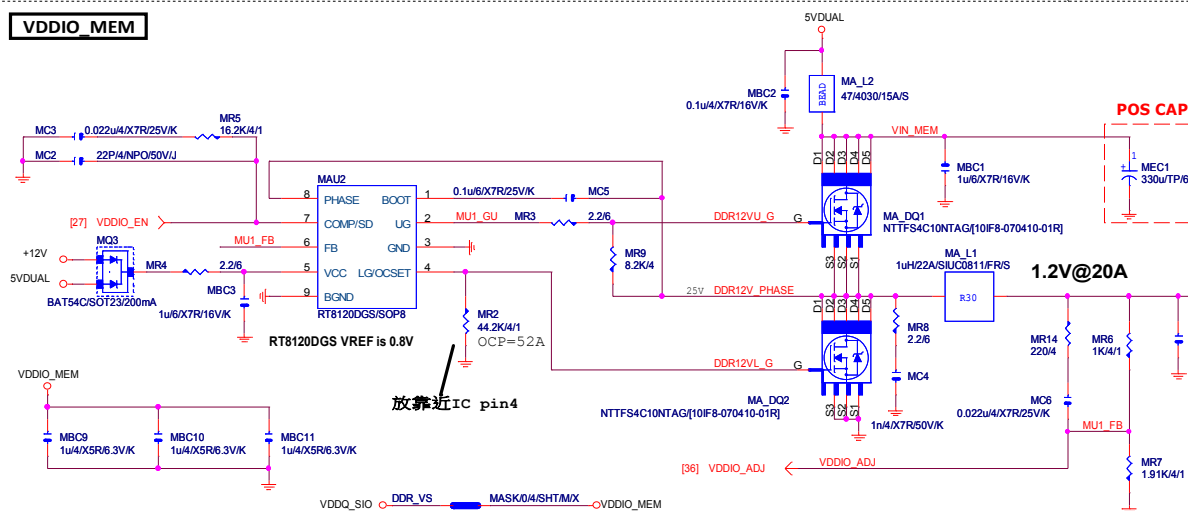
3VDUAL



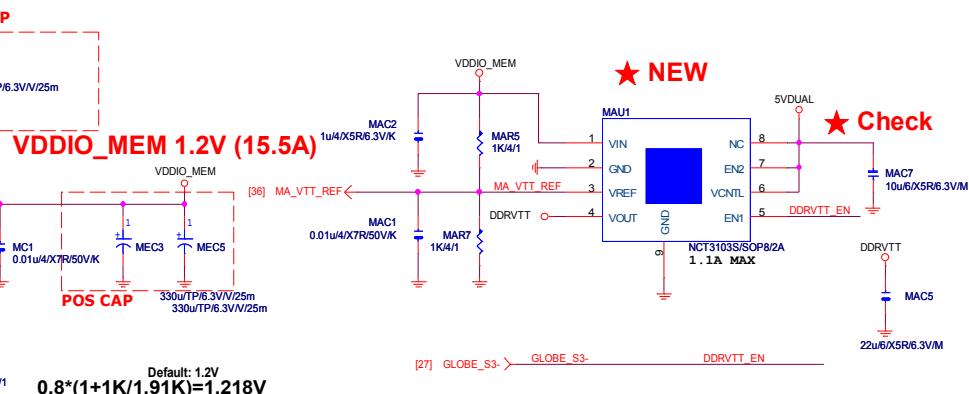
VPP MEM



VDDIO_MEM

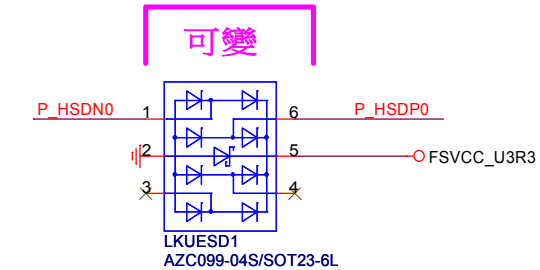


DDRVTT

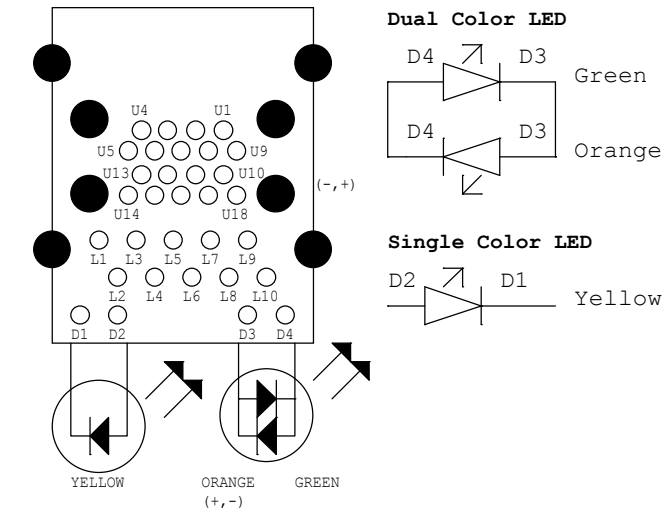


USB_LAN CONNECTOR R0.3

RMA ESD PROTECT



USB30_LAN LAYOUT示意圖

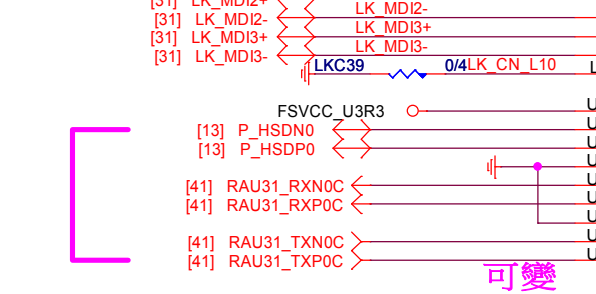


USB_LAN CONNECTOR

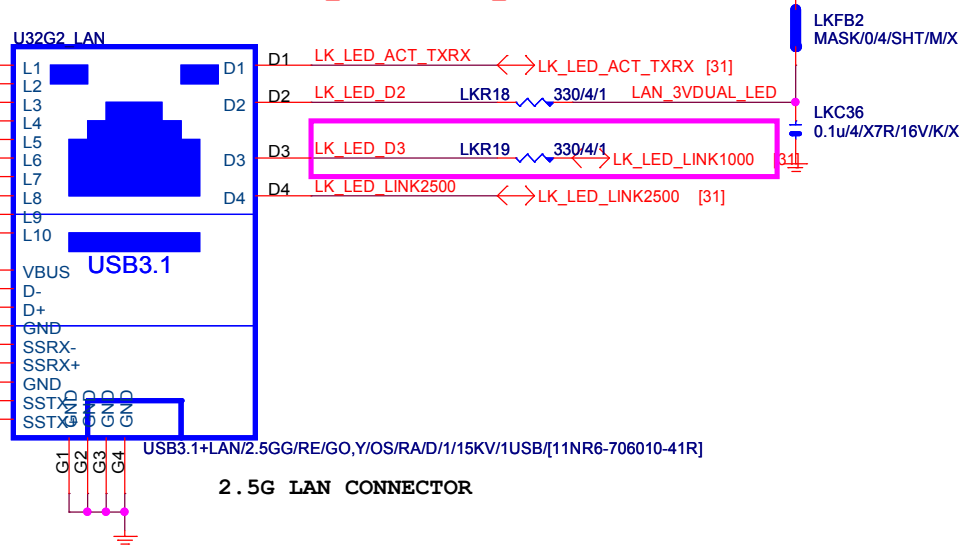
LA_MDI-->100歐姆:[20/4/8/4/20]

For RTL8125B(S)
LKC35 : X

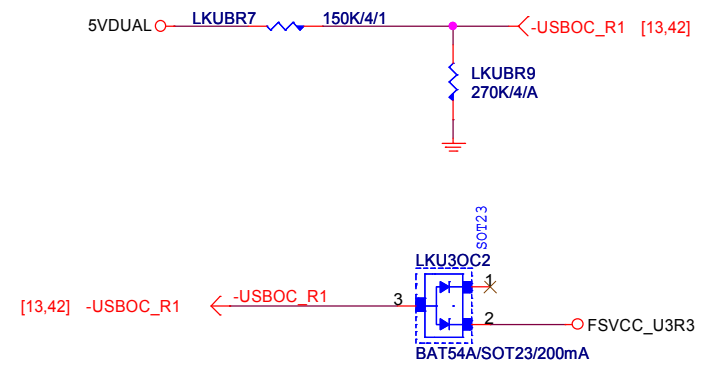
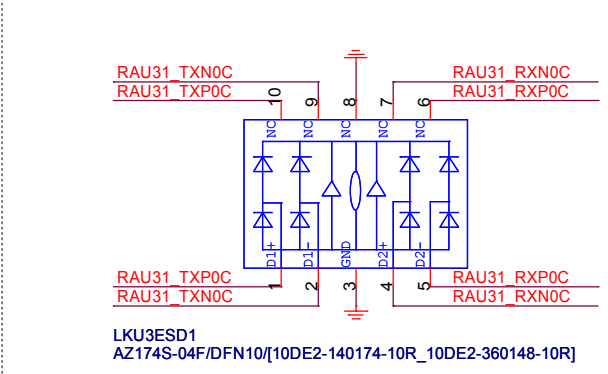
For i219
LKC35 : O



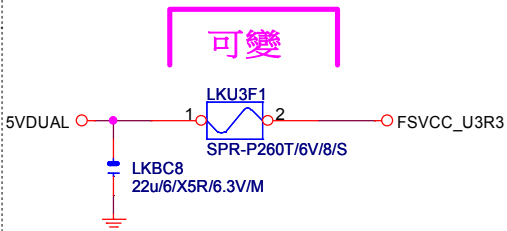
[RTL8125BS] 請依Spec 自行確認USB type
EX: U32_LAN or U32G2_LAN



RMA ESD PROTECT



USB POWER

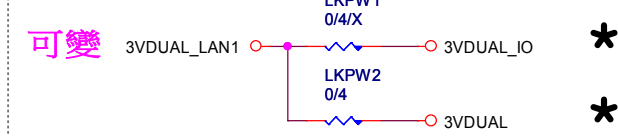


Close to connector
FUSE-0805

EMI SHORT PAD

PS: 視EMI需求

LAN POWER



Gigabyte Technology			
LAN CONNECTOR-RTL8125B(S)			
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Size	Document Number	MODEL NAME	
Custom			
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★Update 2016.06.01

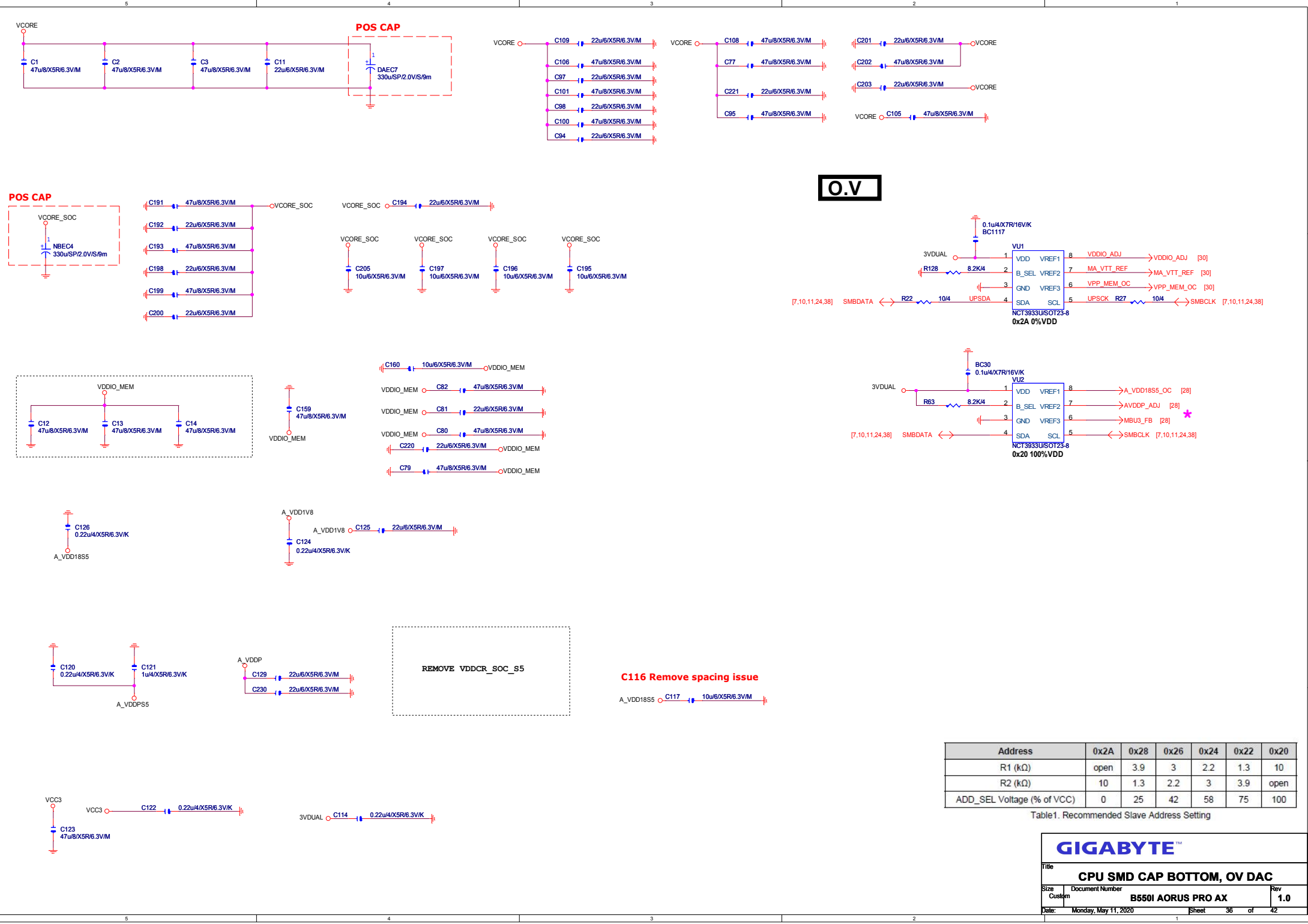


COM PORT

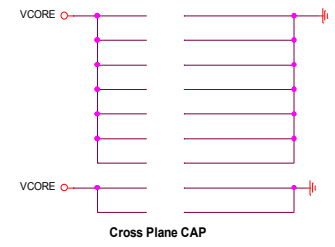
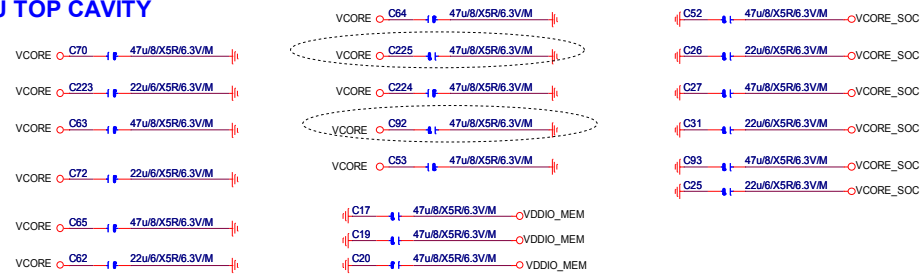
TPM CONNECT



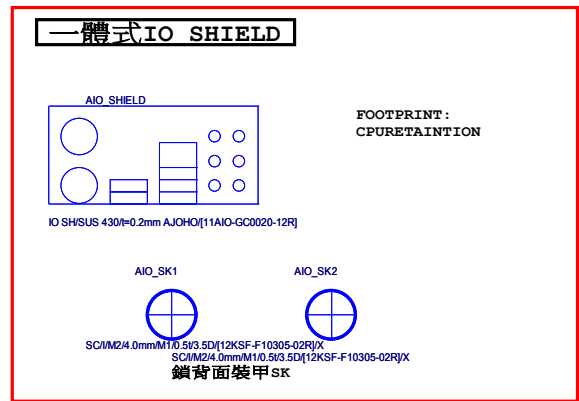
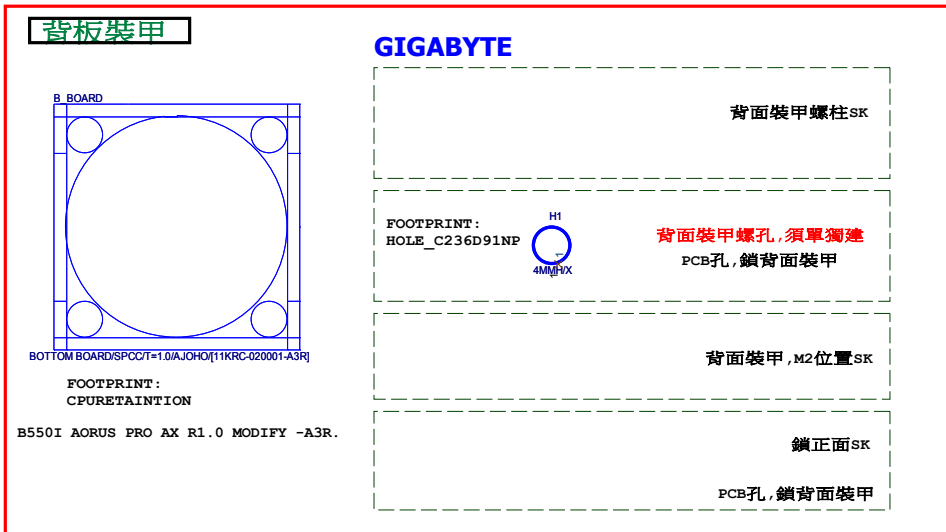
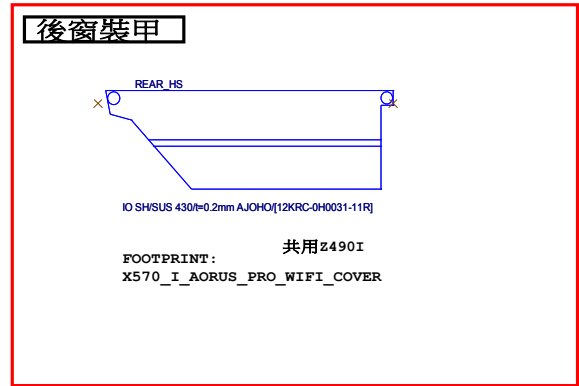
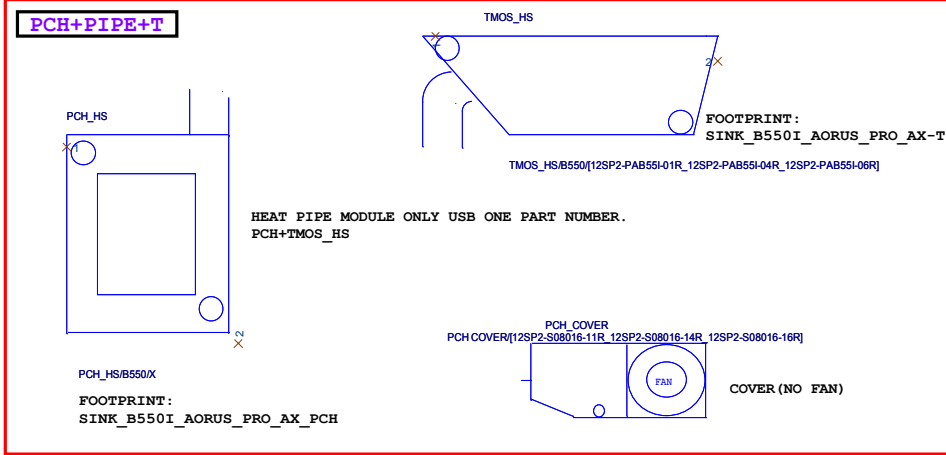
Title			
FAN, LPT, COM ,HWM			
Size	Document Number		Rev
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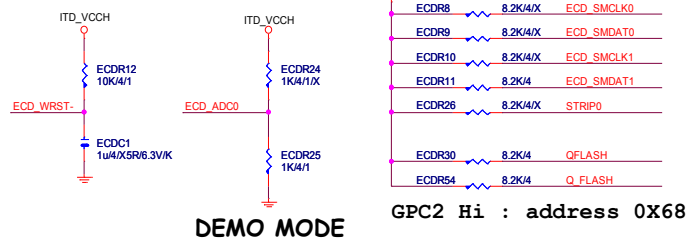
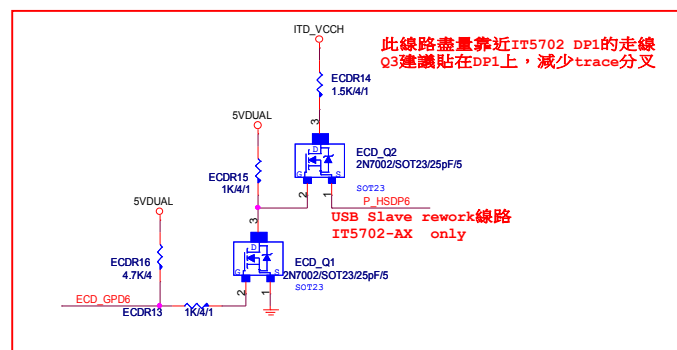
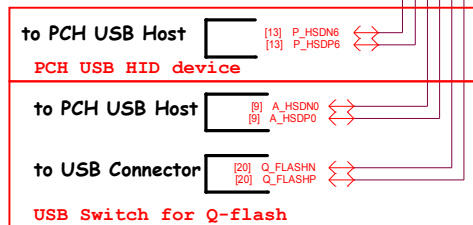
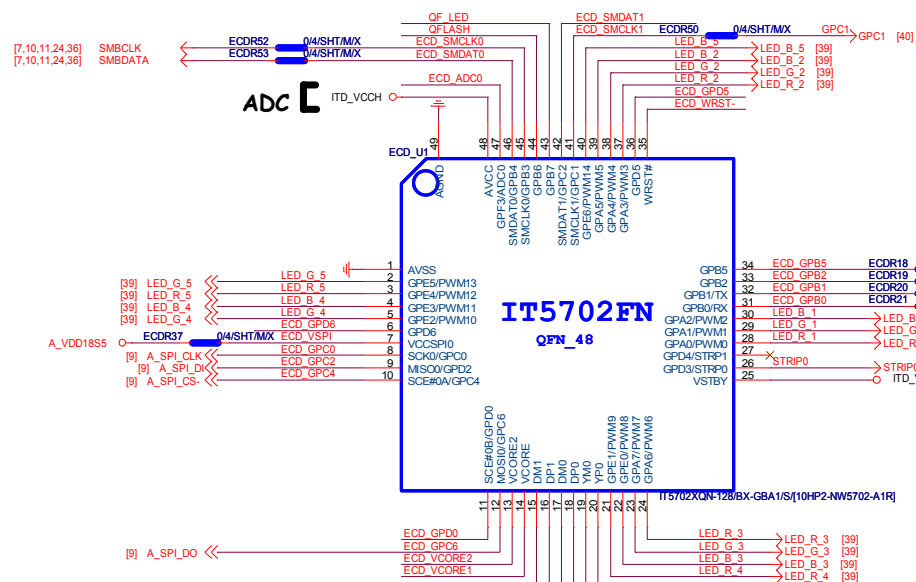


CPU TOP CAVITY

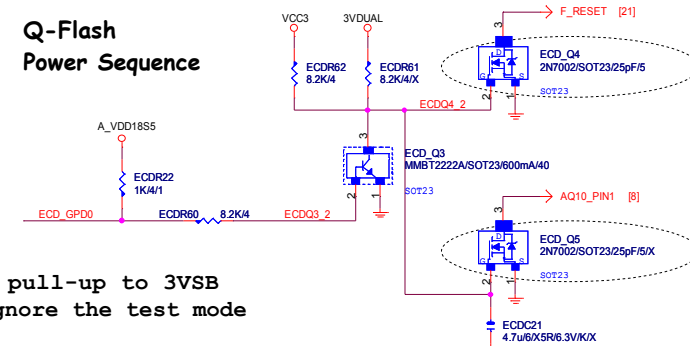


裝甲HEATSINK 分成四大部份



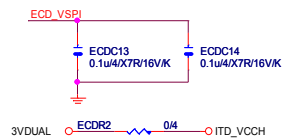
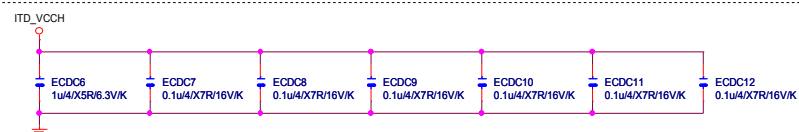
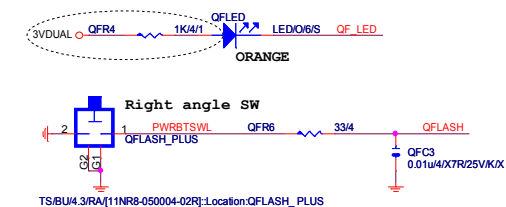


Q-Flash Power Sequence

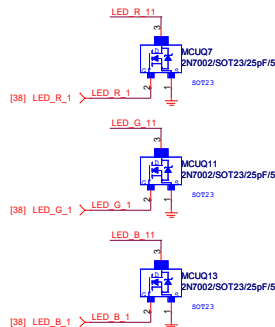
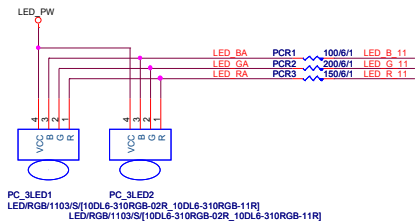


GPD0 pull-up to 3VSB
To ignore the test mode

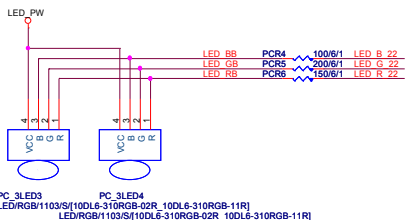
Q_FLASH BUTTON/LED



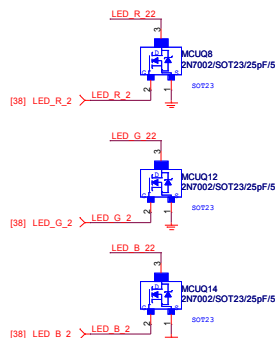
第一區 LED CONTROL



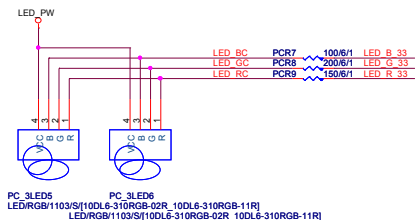
第三區 LED



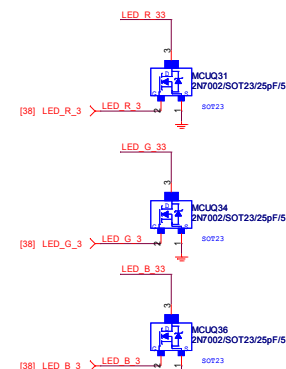
第三區 LED CONTROL



第四區 LED

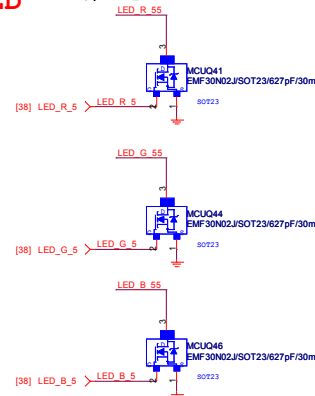


第三區 LED CONTROL

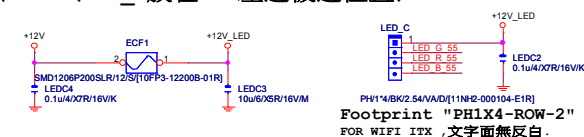


第五區 LED

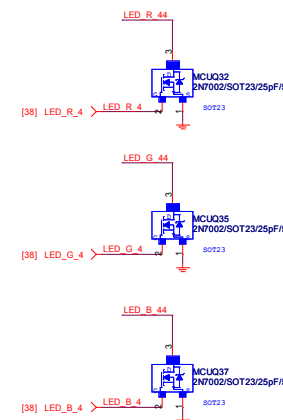
第五區 LED CONTROL



燈條 LED (LED_C放在PCB左邊板邊位置)

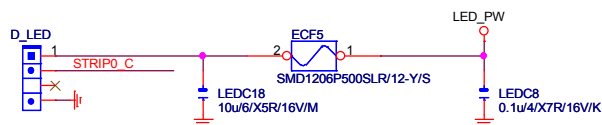


第四區 LED CONTROL



第六區 LED (靠近左上板邊位置)

Digital LED Strip1

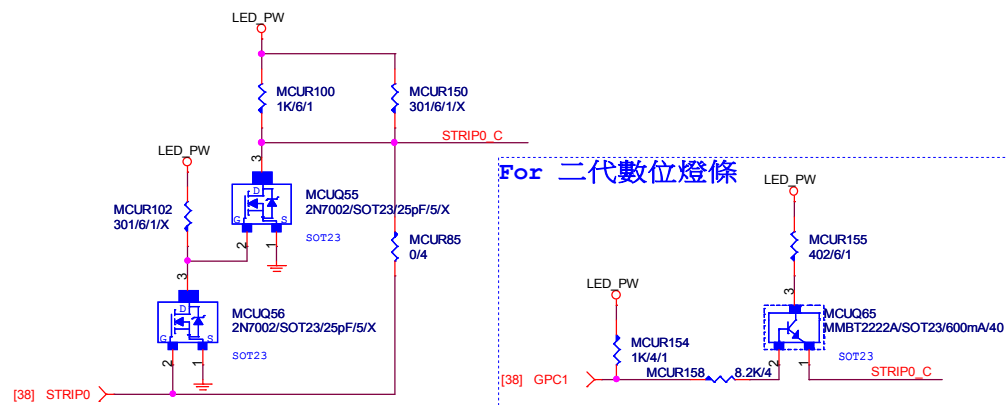


PH1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint "PH1X4-CUT3-LED"

FOR WIFI ITX ,文字面無反白.

燈條 Level shift



GIGABYTE™

Title

D_LED

Size

Document Number

Rev

Custom

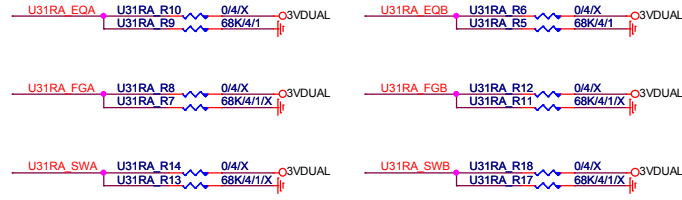
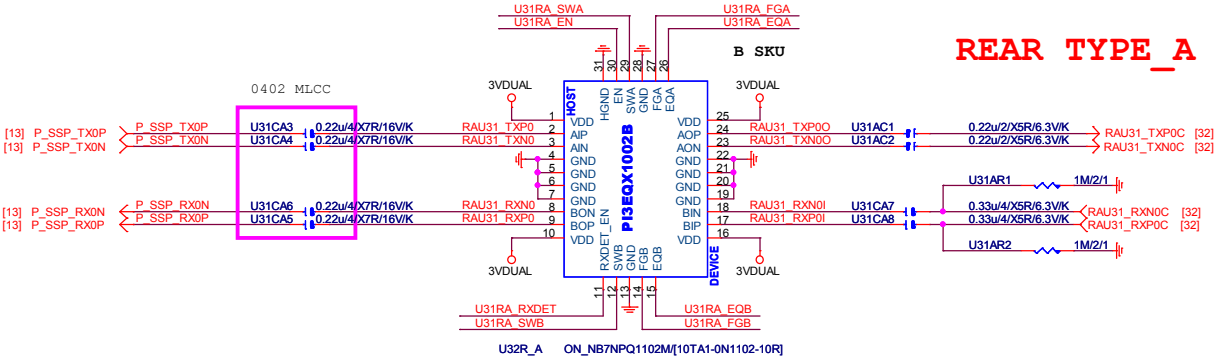
B550I AORUS PRO AX

1.0

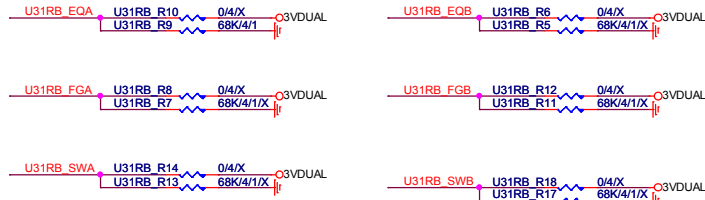
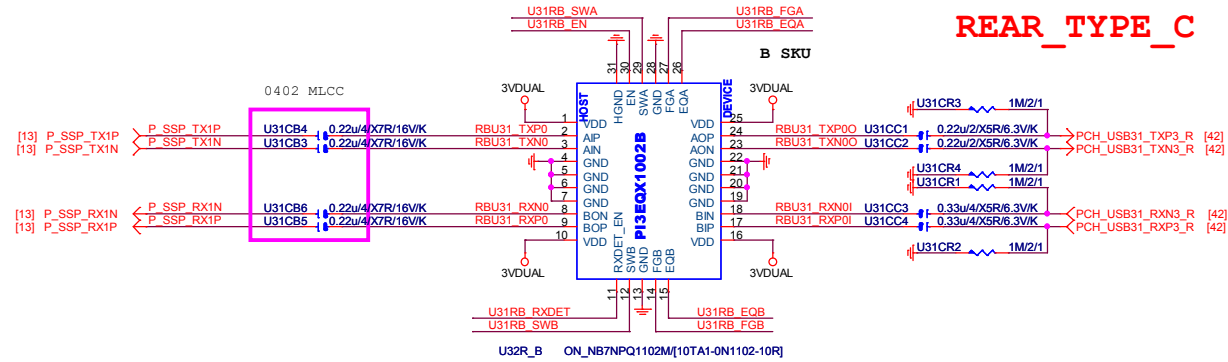
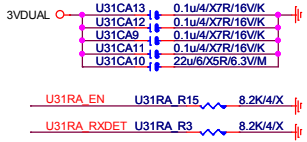
Date: Monday, May 11, 2020

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- Layout Rule:
- 1. Differential Pair can't be swapped
 - 2. Redriver to Connector Length min. 500mil



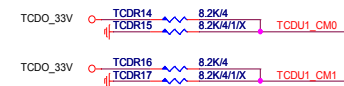
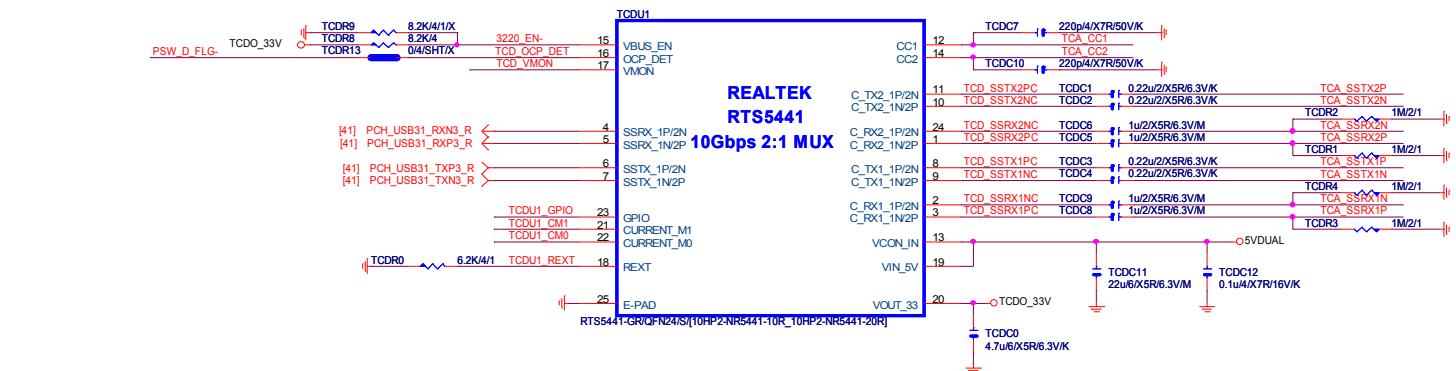
EQA	68K	EQB	68K
FGA	F	FGB	F
SWA	F	SWB	F



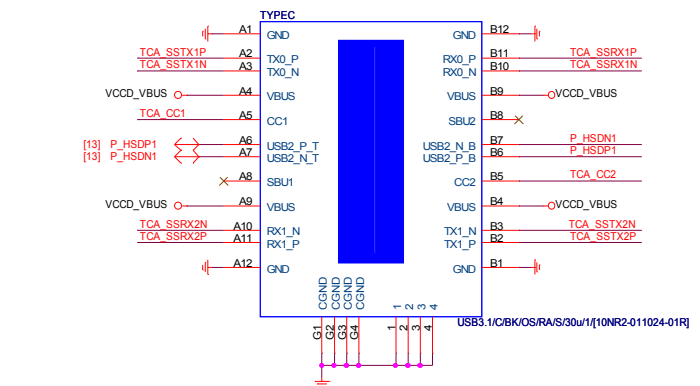
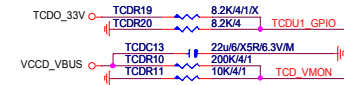
EQA	68K	EQB	F
FGA	F	FGB	F
SWA	F	SWB	F



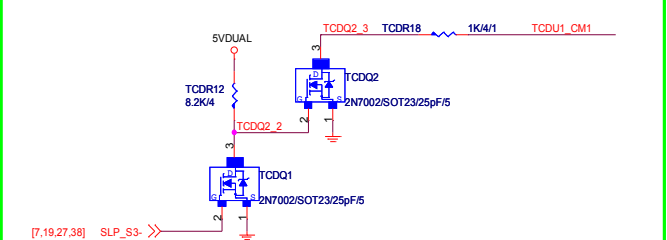
REALTEK CC LOGIC AND MUX RTS5441



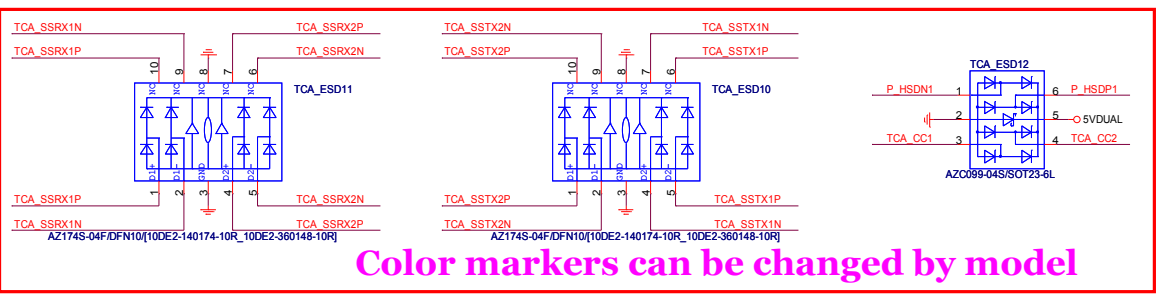
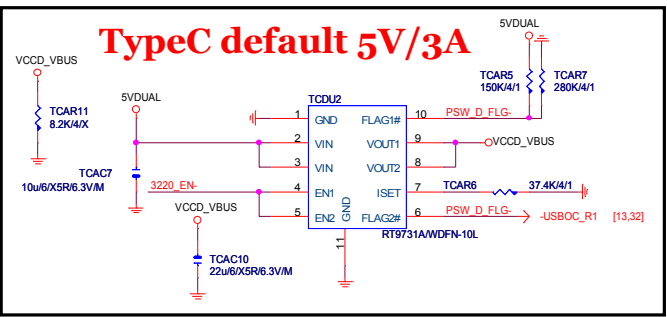
CM1	CM0	Current
0	1	900mA
1	0	1.5A
1	1	3A Default



USB2.0 can be used the same source



For VBUS current limit at 900mA on S3



Color markers can be changed by model